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Design and implementation of high-frequency DC-DC converters for EV applications.

A thesis submitted in partial fulfillment.
The requirement for the degree of
Master of Science in Electrical and Engineering

by

Rahul Biswash
GD Goenka University
Bachelor of Technology in Electronics and Communication Engineering, 2018

May 2024
University of Arkansas

This thesis has been approved for recommendation by the Graduate Council.

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ABSTRACT

The power electronics industry has been revolutionized by introducing wide bandgap semiconductor devices, such as Silicon Carbide (SiC) and Gallium Nitride (GaN). Due to their high frequency, high temperature, and high voltage operating capabilities, wide bandgap devices boast significant improvements in power density, efficiency, and reliability, as evidenced by their ability to decrease the size of power converters by operating at higher frequencies, temperatures and voltages, use of smaller and less passive components, such as transformers, inductors and capacitors, which makes power converters more compact and light-weight, ideal for space and weight-constrained applications, and compatibility with a wide range of power and voltage levels.

GaN offers additional advantages over SiC for low/medium power and medium voltage converters, such as 6 kW and 250 V. For this reason, GaN devices are the preferred choice for low-power converter applications since they can operate at higher frequencies and maintain lower junction temperatures. This thesis proposes designing and implementing a complete bridge power module with GaN HEMT devices for a bidirectional dual active power converter for Electric Vehicle (EV) applications. For that, a suitable bidirectional dual dynamic bridge power converter topology is chosen, justified, and analyzed in detail to design a 5kW power converter.

The modern digital controller implemented in a DSP MCU board is critical for controlling the converter. Based on the testing results, a power loss analysis during operation is carried out and compared with simulation results to evaluate the efficiency and performance of the system designed.

ACKNOWLEDGMENTS

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CHAPTER 1

INTRODUCTION

1.1. Background

With the ongoing progress in electric vehicle efficiency, drawn by the requirement of environmentally friendly solutions, numerous government institutions are partnering to generate sustainable technology meant to reduce carbon emissions, driving innovation with power electronics in the middle of it. The power system architecture is growing extremely complex to meet the new requirements of this increasingly intricate landscape.

Power converters have gone from simple devices hard-pressed by physical requirements to reach higher and higher density to highly sophisticated systems that must operate in very close spatial confinements to attain it. This need for density demands high-frequency designs, bringing more significant and complicated problems to the designers. This complexity underscores the intricate nature of modern power systems and their critical role in advancing sustainable transportation solutions. [1]. Due to the demand for high-density power converters and EV chargers, it is now moving toward high-frequency designs. A typical architecture of modern onboard EV chargers, as shown in Figure 1.1, consists of the proposed bidirectional dual-active converter.

This thesis focuses on designing Isolated bidirectional DC-DC converters using a dual active bridge topology, which is familiar within power electronics. The DAB configuration utilizes ZVS (Zero-Voltage Switching) operation to maintain the power converter's overall performance and stability. On the other hand, research has been done to improve power efficiency, power density compatibility, and other functionalities by developing a new GaN-based power module that can

work at high frequency to meet the application requirements.

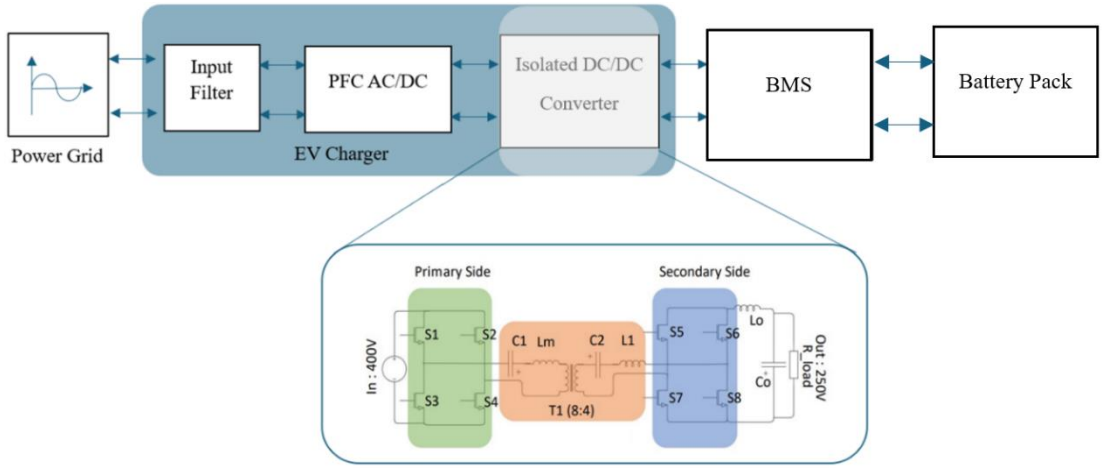


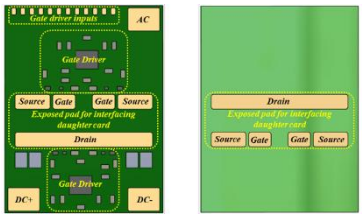
Figure 1.1: Architecture of onboard EV charger

1.2 Previous Work

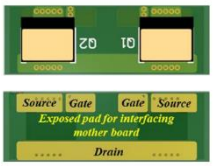
The power modules based on SiC and GaN are widely used to design power converters due to their Wide-band gap nature, high speed, and high efficiency. On the other hand, GaN HEMT (High electron mobility transistor) operates at an Mhz level frequency compared to its counterpart SiC due to its very high carrier mobility. Previous work considering these performance matric GaN-based modules over SiC have been reviewed and fabricated half bridge 650V/50A Baseline GaN module. The whole structure is based on the review of electromechanical performance and reliability standpoint. In the design of this module, the gate driver and power routing consist of identical PCBs. Two of the GaN (GS66516) system prepackaged devices are added in parallel to each other to increase power density. The placement of devices and DBC is optimized on both sides. Previous work refers to thesis work. [2]

Minimum thermal coupling and maximum heat spreading with very low stray capacitance from the switching node to the ground, further limiting the CM and DM EMI emissions. The PCB layer is optimized to avoid coupling between the gate and the power loop. The decoupling capacitors

are integrated inside the module along with the SI8271 gate driver in the module. Still, due to a height mismatch between the device and capacitors, it was impossible to attach the DBC pad. Therefore, to address this problem, two PCB spacers (daughterboard) were added to each side. Figure 1.2 (a) and (b) show the PCB of the designed module.



(a) Top and bottom view of module



(b) PCB spacers

Figure 1.2. CAD model of the previous module

The Fig. 3 exploded view of the designed module's CAD model shows the placement of DBC thermal pads on the top/bottom sides of the module. The DBC pattern was also optimized to minimize the stray capacitance and maximize the heat flow. This feature enhances thermal management by ensuring that heat generated within the module can escape from a more significant number of surfaces and improves the reliability and performance of the module overall—figure 1.4 picture of the fabricated module.

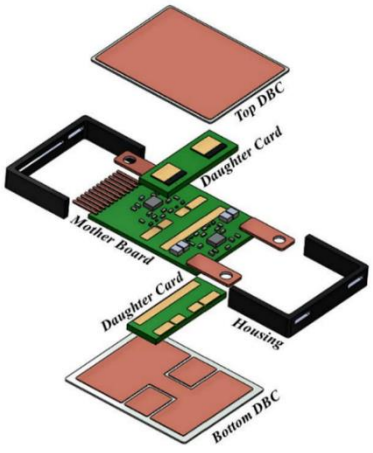


Figure 1.3 Exploded view of the module's 3D CAD model.

Figure 1.4: Fabricated module.

1.3 Stating the Problem

The proposed thesis targets a DC-DC converter for the EV application. Half-bridge and full-bridge configurations are commonly used to design DC-DC converters for many applications. Each configuration has its advantages and disadvantages, case to case. The above design module is a multichip half bridge with paralleled power devices, and the maximum current stress can be 120A. The proposed Converter 30A maximum current is needed to be capable of one device. The above module design is suitable for high current density but, at the same time, is a bit space-consuming as one single module device is a multichip half-bridge, and the proposed converter is fully bridge-based. Therefore, a new module, a full bridge and single chip, has been developed based on the requirements inspired by the above design. The new module design includes a compact, thermally efficient bridge topology with a short power and gate driver loop of all auxiliary circuity within the module.

1.4 Objective

This thesis aims to design and implement high-frequency DC-DC converters for EV applications, where a phase-shifted switching frequency is used to operate the Gallium Nitrite (GaN) Power switches. A new GaN-based full bridge Power Module will be designed and implemented with galvanic isolation using a high-frequency (Payton Transformer) for the proposed converter design. Several computer simulations will use the same switching strategy to meet the design requirement. Then, a hardware prototype of the converter will be designed to evaluate and analyze its functionality and efficiency, which includes the DSP programming integrated with the PI controller.

1.5 Thesis organization

This thesis is organized in the following way: Uses of GaN in high-frequency power converter design in EV onboard charging application and its literature review discussed in Chapter 2, The down architecture of the bidirectional DC-DC power converter, analysis of power flow, and selection of transformer and leakage inductance is described in Chapter 3, Designing New GaN module and DPT testing includes in Chapter 4, Simulation, design consideration of converter and Implementation of the circuit with DSP coding done in chapter 5, finally, Chapter 6 concludes the thesis.

CHAPTER 2

LITERATURE REVIEW

2.1 Comparison of GaN with SiC and Si

The wide band gap devices, like silicon carbide (SiC) MOSFETs and gallium nitride HEMTs, are widely used in power electronic converter design due to their material features like broader band gap, faster mobility of electrons, lower switching losses, high critical field, higher operating temperature, etc. On the other hand, silicon (Si) based power MOSFETs/IGBTs have limitations. Due to stronger bonds in the lattice of semiconductors, more energy is needed to jump electrons from the lower band to the higher conduction band, which ultimately tends to smaller leakage currents and higher operating temperatures [3]. Table 1-1 [1] shows [4] The salient features of WBG devices align well with the future of power electronics converter applications.

Parameters	(Si)	SiC	GaN
Band Gap E_g (eV)	1.12	3.25	3.4
Critical Field E_{Crit} (MV/cm)	0.23	2.2	3.3
Electron Mobility (μ_n) (cm^2 $/V.s$)	1450	950	1500
Permittivity ε_r	11.8	9.7	9
Thermal Conductivity λ $(W/cm.K)$	1.5	3.8	1.3

Table 2.1 Material properties of Si, GaN, and SiC [1]

The stronger bonds in WBG devices cause higher critical field energy, as shown in the above table, and the drift region (W_{dift}) is approx. Ten times smaller in WBGs than Silicon, which further gives breakdown voltage V_{BR} as shown in equation 2.1 and higher electron concentration.

$$V_{BR} = \frac{1}{2} w_{\text{drift}} E_{\text{crit}} \tag{2.1}$$

The number of electrons can be calculated using Poison's equation (2.2) between two terminals. Due to the smaller drift region, the critical electric field E_{crit} becomes ten times higher, leading to a higher density of electrons in the drift region.

$$N_D q = \frac{\varepsilon_0 \varepsilon_r E_{\text{crit}}}{w_{\text{drift}}} \tag{2.2}$$

In equation (2.2), q is a charge on the electron, N_D Is the electron number, ε_0 is the permittivity in a vacuum, and ε_r is the material's relative permittivity. Using the above material properties, the resistance of SiC and GaN devices can be calculated using the equation below 2.3 or 2.4.

$$R_{on} = \frac{w_{\text{drift}}}{N_D q \mu_n} \tag{2.3}$$

$$R_{on} = \frac{4V_{BR}^2}{\varepsilon_0 \varepsilon_r \mu_n E_{crit}^3} \tag{2.4}$$

It is found that both SiC and GaN have low on-resistance, and farther GaN devices show significant advantages in terms of smaller die size and die capacitance, which further contributes to higher switching frequency operation with fewer [5].

Due to the popularity of GaN devices over their counterparts to SiC, many semiconductor industries are now manufacturing GaN devices and modules. The most popular one is rated 600-650 V due to its EV and solar inverter application. The use of GaN devices in power systems offers fast switching with significantly reduced switching losses, which gives high efficiency compared to its counterpart's design. In the automotive and future, the electric aircraft application of GaN can be a game changer due to its lightweight and fast switching ability, where power density plays a

crucial role. GaN is the best choice for high-frequency power converter design, where size is significant. Fast switching can reduce the size of the components, such as inductors, input and output capacitors, and isolated transformers. Reduced switching losses lead to a small heat sink; therefore, GaN is a good choice for onboard charger design.

In recent research [5], GaN System Inc. compared GaN E-HEMTs and SiC MOSFETs for DC-DC synchronous buck-boost applications. They found that GaN devices offer more efficiency in power conversion at higher frequencies due to their lower internal capacitance and almost zero reverse recovery charges. They chose the GaN system's GaN E-HEMT GS66508T and Cree SiC MOSFET C3M0065090J to demonstrate this approach. The electrical characteristics of the two devices are shown in Table 2.2 below.

Parameter	GaN E-HEMT GS66508T	Cree SiC MOSFET C3M0065090J
Package	Low Inductance GaNPXTM D2PAK	D2PAK
VDSmax	650 V	900 V
ID@25°C	30 A	35 A
VGS	-10/+7 V	-4/+15 V
RDS(on)@25°C	50 mΩ	65 mΩ
Ciss	260 pF	660 pF
Coss	65 pF	60 pF
Crss	Two pF	4pF
Qg	5.8nC	30.4nC
Qgs	2.2 nC	7.5 nC
Qgd	1.8 nC	12 nC
Qrr	0 nC	245 nC

Table 2.2 Electrical Characteristics of GaN E-HEMT and the SiC MOSFET

These devices were used to build a half-bridge, and a hard-switching double pulse test was conducted. The $\frac{dv}{dt}$ of the GaN devices were four times faster in the turn-on period than SiC. On the other hand, the $\frac{dv}{dt}$ during the turn-off period, the GaN devices were found to be two times faster than those in SiC.

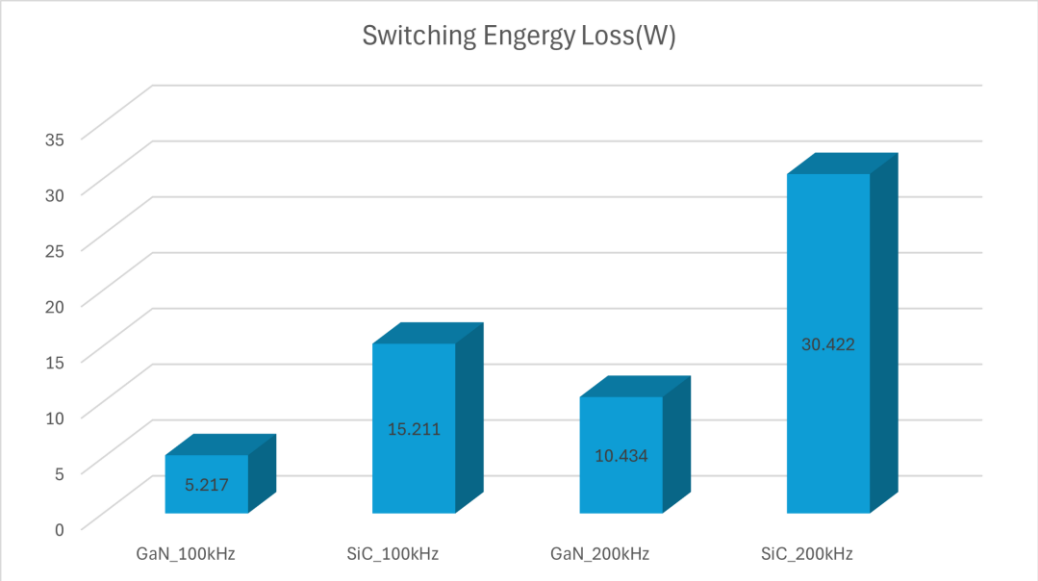


Figure 2.1: Losses in GaN and SiC at different frequency

On the other hand, using the same test condition, GaN devices show much more improved E_{on}/E_{off}. This E_{on}/E_{off} is used to calculate the switching losses, for example $(E_{on} + E_{off}) \times f_{sw}$ where f_{sw} is the operating frequency. In this demonstration, the switching loss of GaN is 5.217 W, and for SiC, it is 15.211 W at 100 kHz. At 200 kHz, the power switching losses of GaN are 10.434 W, and SiC is 30.422 W. The GaN device shows significant improvements and saves 10W at 100khz and 20 W at 200kHz, respectively, over its counterpart SiC devices; the figure above shows the results.

The above demonstration shows that in high-frequency synchronous buck-boost DC-DC converter application, the GaN device shows much higher efficiency than SiC devices in terms of

performance and heat sink design, which helps the engineer to design a more power-dense and efficient power converter. The 650 V GaN devices in commercial employment have become highly favored, given their low channel resistance, enabling a high current capability, minimal capacitive parasitic, and reversal recovery charge exemption. Each of these aspects significantly contributes to enhancing efficiency and power density and enabling higher switching frequencies. As a result, the size of magnetic components, such as the previously bulky high-frequency transformer typical for the DAB topology, has significantly decreased. On the other hand, they realize the advantages listed, which results in new design problems. The increased di/dt and dv/dt values require the correct layout to avoid long inductive loops relevant to an optimal signal and ground plane arrangement. Moreover, proper component choice enabling effective mitigation of stray inductances is also highly essential due to the high-frequency mode of operation.

2.2 Review of EV charging design

The rapid consumption of fossil fuels raises concerns about growing $\mathbf{CO_2}$ emissions and greenhouse gases, leading causes of global warming and air pollution. At the same time, the depletion of fossil fuels ultimately pushes the energy sector and car industries to develop eco-friendly and sustainable technologies. For this reason, electric vehicles have become very popular worldwide in the last few years. This demand for EVs worldwide also raises the demand for reliable access to charging infrastructure, wall chargers, and onboard chargers. EV battery chargers can be classified based on their power rating, for example, level 1, level 2, and level 3, as shown in Figure 1.1. EV chargers can be unidirectional or bidirectional power flow [6]. In a bidirectional charger, power can flow from girl to vehicle and from vehicle to grid (in the reverse direction), which can be used as backup up generation and supply power back to the grid whenever needed; it is a reliable

approach to preventing system failure in case of peak load and unexpected conditions. In the long run, this approach of powering the grid from vehicles can reduce the cost of power generation; therefore, this is a trending research area.

Power Level	Charger Location	Typical Use	Typical Power	Charging Time
Level 1	On-board	Home	< 2 kW	4–11 hours
Level 2	On-board	Public	2- 20 kW	1– 4 hours
Level 3	Off-board	DC Fast	20- 100 kW	< 30 minutes

Table 2.3 Power Level of EV charger [7]

2.1.1 Onboard Charger

EV chargers can be implemented inside or outside the vehicle; onboard chargers (OBCs) are limited to their size and weight as installed inside the vehicle. Because of this, this kind of Charger is known as a level 1 or level 2 charger. The architecture of an onboard charger is shown in Figure 1. There are two stages inside the charging system, initially the AC-DC stage and then the DC-DC stage. In the first stage, the Charger consists of a rectifier and power factor correction (PFC), which works as an input filter and lowers the harmonic distortion from the grid, resulting in less electromagnetic interference (EMI) in the Charger. The rectification can be achieved with the combination of diodes and active switches. Bidirectional power flow can be done by replacing all diodes with active switches. [4].

The second stage is followed by the first stage, consisting of an isolated DC-DC converter. Galvanic isolation is required for safety, which means the battery pack, battery management system (BMS), and vehicle internal circuitry must be isolated from the primary power source and AC grid. Resonant converters are commonly used in this stage. The main reason for using resonant power converters is that they allow very high frequency with ZVS or ZCS and lower switching losses;

these two parameters are essential to achieve high density in the power converters.

2.2.2 Offboard Charger

An offboard, or a level 3 charger, has a higher power rating and is commonly installed outside the vehicle. For example, it can be wall-mounted, charged in the parking area, or charged in a charging station. The fundamental block of the electric vehicle infrastructure used in offboard charging is a system that has a complex structure to efficiently pass power from the grid into the vehicle's battery. The base of such a system is designed according to strict safety and performance regulations, and galvanic isolation is a must, according to the IEC EN 61,851–23. The first block of the EV infrastructure is the grid-facing AC/DC converter, which converts AC voltage from the grid to DC voltage. The second block of the system is the DC/DC converter, which further provides an interface to the EV battery. Depending on the converter topology, the two stages of the off-board charging system can support unidirectional or bidirectional power flow. Unidirectional flow occurs when the EV battery is charged from the grid. Bidirectional flow ensures energy exchange between the vehicle and the grid. The figure shows the architecture of an offboard charger [8].

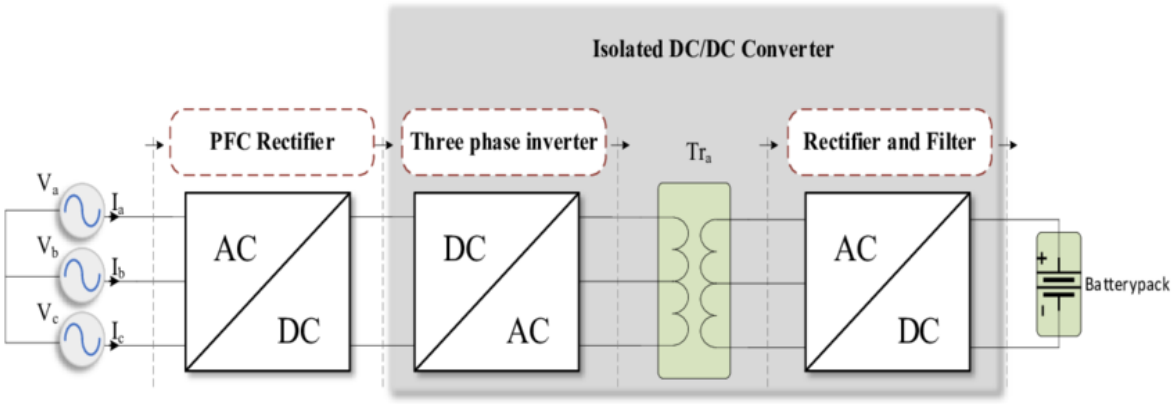


Figure 2.2 Architecture of offboard charger

CHAPTER 3

CONVERTER ARCHITECTURE

3.1. Top-Down Architecture of Bidirectional DC/DC Power Converter.

The converter topology had to be simplified and power efficient under high operating frequency. On the other hand, bidirectional power flow is required. The review of various topologies above found that the isolated dual active bridge (DAB) converter with CLLC configuration meets the design requirements. Although the CLLC converter can be considered more efficient and advanced in light-load handling than DAB, the latter remains a highly competitive rival. DAB systems benefit from better performance, as they are better in terms of a lower component count. Additionally, their control is more straightforward, as it involves fixed switching frequencies, and they offer a broader range of output voltages, allowing them to adapt to more types of batteries [9]. At the same time, the market is gradually turning to wide-bandgap technology, which uses SiC or GaN rather than traditional Si devices, which leads to the diminishing popularity of the conventional Si converter. In the proposal design, an isolated bidirectional DC/DC converter and topology is a dual active bridge used due to using eight semiconductor devices in a dual active bridge, the high-frequency transformer, and input and output dc-link capacitors and energy transfer the inductor. The two full bridges operate at a fixed switching frequency and a 50% duty, and the power flow is controlled by modulating the voltage on the series inductor, controlled by the phase difference of the gate signals of the two full bridges. In this symmetric scheme, the power flow is bi-directional. Moreover, the converter allows a wide range of voltage generation, either in a buck or boost mode, by the imposition of the sum and the difference of the input/output voltage across the inductor.

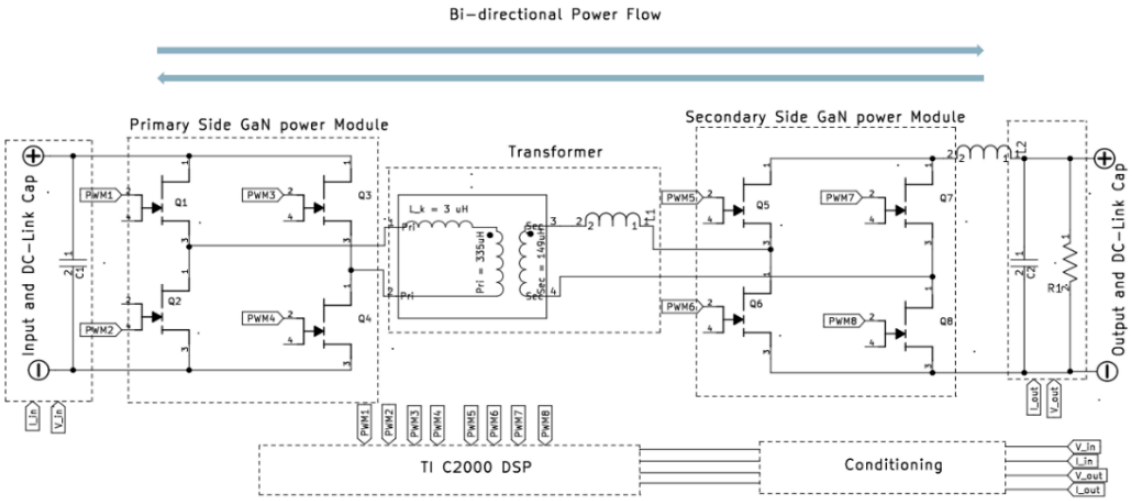


Figure 3.1. Architecture dual active bridge

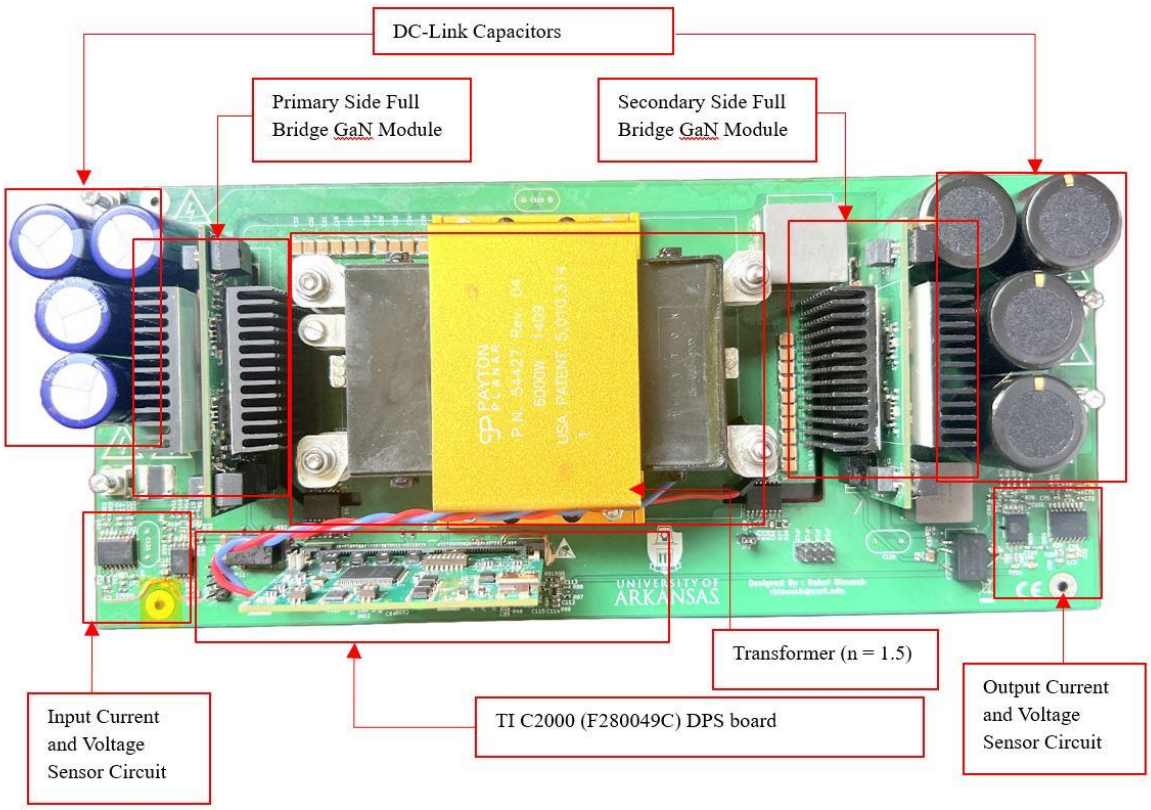

DC-Link Capacitors
Primary Side Full Bridge GaN Module
Secondary Side Full Bridge GaN Module
Transformer (n = 1.5)
Output Current and Voltage Sensor Circuit
TI C2000 (F280049C) DPS board
Input Current and Voltage Sensor Circuit

Figure 3.2 Top view of implemented dual active bridge circuit.

A typical schematic of a dual-active bridge is shown in Figure 1.1. Note that and are the DC link voltages, and L is the transformer leakage inductor, which needs the assistance of an external energy transfer inductor. C1 and C2 are input and output DC link capacitors essential in stabilizing the input and output voltages. The switches used are GaN HEMTs, which can conduct in the 3rd quadrant [11] without an external anti-parallel diode and operate under ZVS conditions. On the other hand, SiC switches use anti-parallel diodes for the ZVS operation of the converter design [10]. TI C2000 DSP board controls the GaN switches using phase shift PWM signals conditioning with input and output feedback signals. Figure 3.1 shows an actual picture of the implemented dual-active bridge circuit.

3.2 Power Flow Analysis

The functionalities and workings of a dual active bridge converter can be explained with the help of a power flow analysis between two AC sources, as the isolated transformer works in AC signals, and second, the generation of a square wave AC signal from a DC source using an H bridge. The dual active bridge (DAB) converter utilizes AC power to transfer energy from the primary to the secondary side through a transformer [12]. The direction of power flow is changed by controlling the phase shift between two AC sources, which can be understood from the explanation below. The figure below shows two AC sources. Here V_1 and V_2 are the two AC voltage with the θ_1 and θ_2 Phase angles of respective sources.

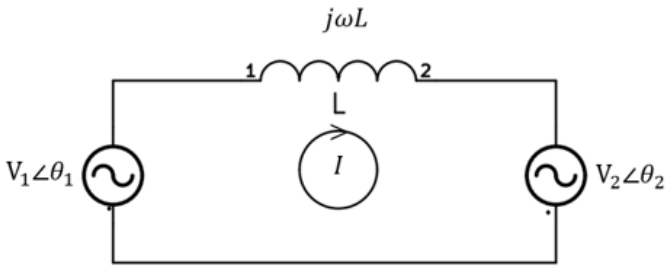


Figure 3.3. Circuit of power flow between two AC sources.

Initially, the reference phase angle is θ_1 is zero, and the phase difference between the two sources is θ_2 . A phasor equation (3.1) can represent the loop current in the above figure.

$$\bar{I} = \frac{V_1 \angle \theta_1 - V_2 \angle \theta_2}{j\omega L} \tag{3.1}$$

The above equation can be represented in the time domain.

$$I(t) = \frac{V_1}{\omega L} sin\ (\omega t) - \frac{V_2}{\omega L} sin\ (\omega t - \theta_2) \tag{3.2}$$

The power on the secondary side can be expressed using the value $\boldsymbol{I(t)}$ from the above equation.

$$P_2(t) = V_2(t) \cdot I(t) = V_2 \cdot \cos\ (\omega t - \theta_2) \left[\frac{V_1}{\omega L} \text{Sin}\ (\omega t) - \frac{V_2}{\omega L} \text{Sin}\ (\omega t - \theta_2)\right] \tag{3.3}$$

Averaging the power over one period can be represented as Ts, which leads to simpler equations.

$$P_{2,\text{ average}} = \frac{1}{T_S} \int_0^{T_S} P_2(t) dt \tag{3.4}$$

After putting equation (3.3) in (3.4) and integrating it leads to equation (3.5)

$$P_{2,\text{ sine}} = \frac{V_1 V_2}{\omega L} \text{Sin}\ \theta_2 \tag{3.5}$$

The above equation is a power transfer equation where the phase θ_2 determines power flows in dual active topology. If the phase θ_2 is positive, then energy will flow from V_1 to V_2; on the other hand, if the phase θ_2 is negative, energy flows in the opposite direction from V_2 to V_1.Power transfer by changing the phase angle needs an inductor. Here, the leakage inductance of the transformer plays a critical role. The DAB converter utilizes square waves instead of sine waves, but the same principles are at work.

3.3 Working of Dual Active Bridge.

In a Dual Active Bridge, the primary bridge acts as an inverter, the secondary side bridge works as a rectifier, and the phase shift flows the power, as explained before. Phase shift PWM signals are applied to control primary and secondary side bridges, as shown in Figure 3.4. Power devices are divided into pairs in a full bridge, as shown in the figure. These pairs operate complementary modes with the same switching frequency, 50% duty cycle, and some dead time and cycle period Ts.

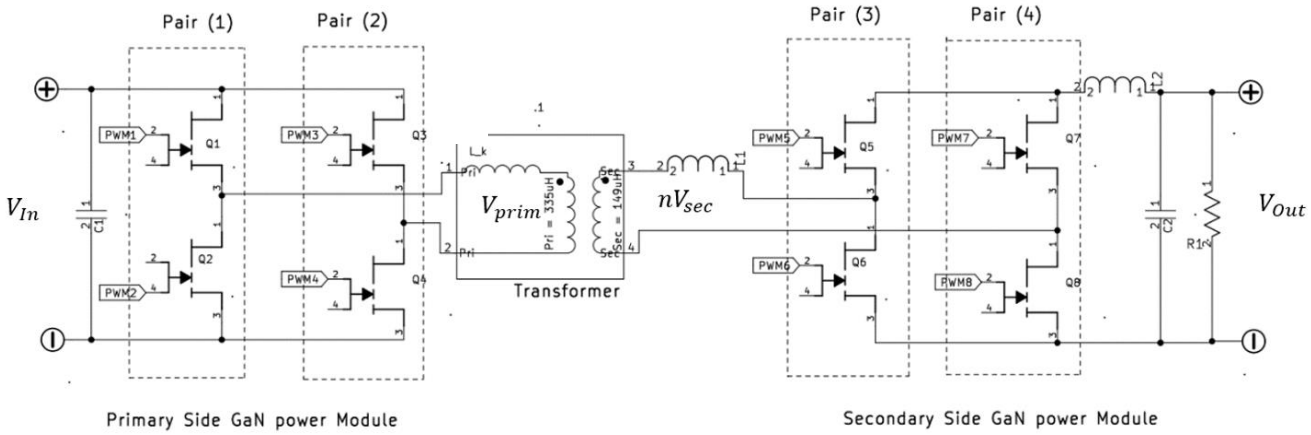


Figure 3.4. Complementary switching pairs in dual active bridge

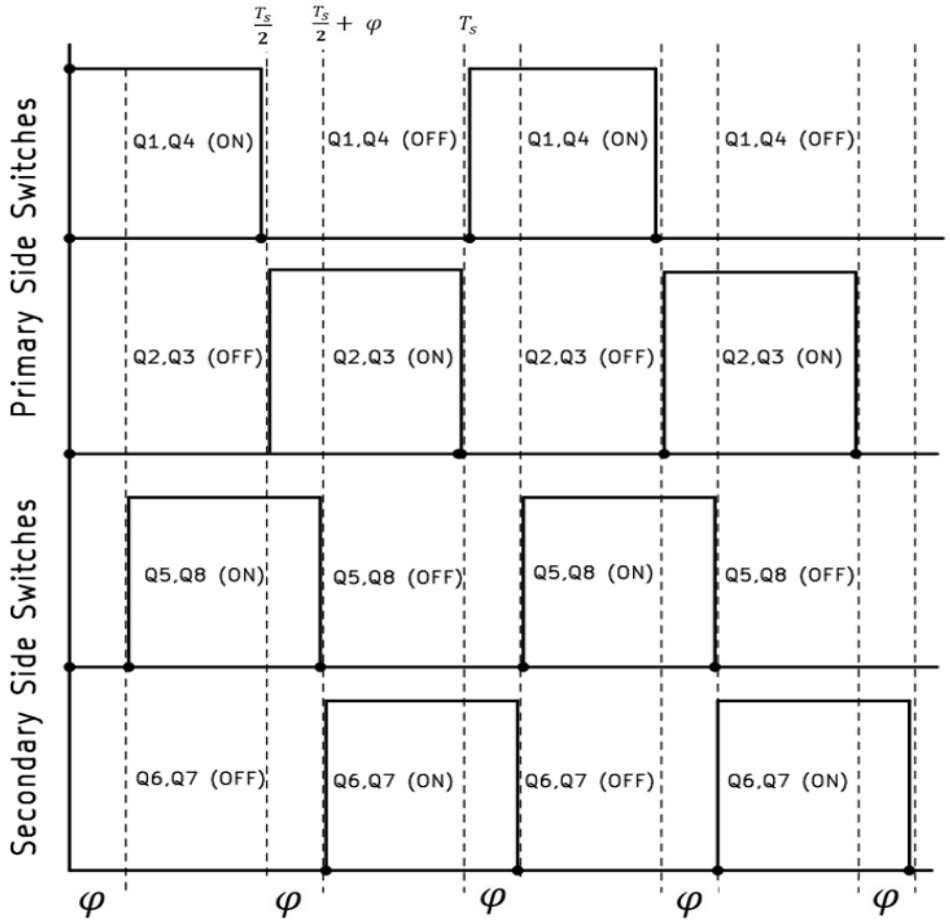


Figure 3.5 Phase-shifted PWM signals.

The current through the transformer's leakage inductance is responsible for the power flow in the converter, and it depends on V_{prim} , V_{sec} , Leakage Inductance, and Phase shift, as shown in equation (3.5). The current through the inductor is a function of inductor voltage and self-inductance, as shown in equation (3.6) and (3.7). On the other hand, the voltage across the inductor is the difference between the transformer's primary and secondary side voltage and is divided into four intervals.

$$L\frac{di_L(t)}{dt} = V_L(t) \tag{3.6}$$

$$L\frac{di_L(t)}{dt} = V_1(t) - V_2(t) \quad where\ 0 < t < \frac{T_S}{2} \tag{3.7}$$

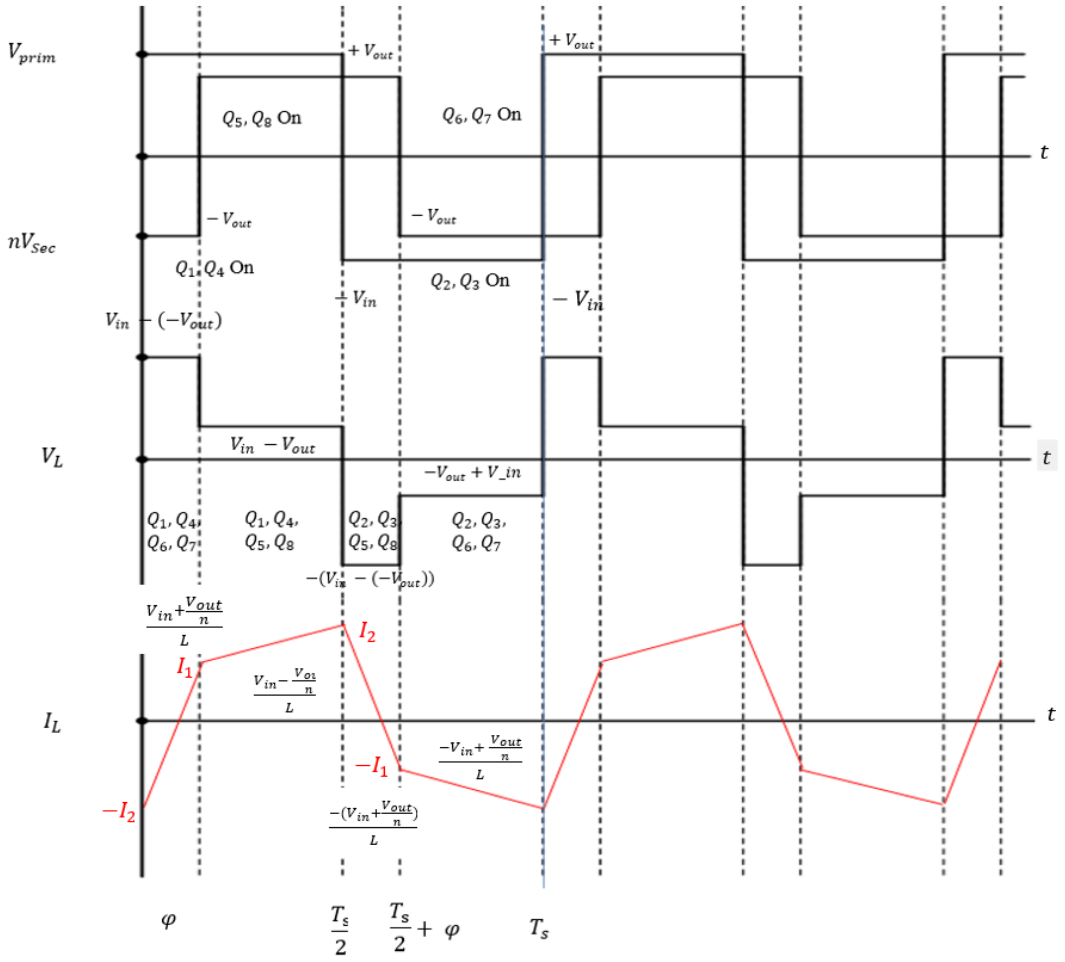


Figure 3.6. The primary side is the secondary side of the transformer voltage, and the inductor voltage and current waveforms.

Considering the operation of the dual active bridge in ideal conditions (no losses), on the primary side, in the first half, at the period $\frac{T_s}{2}$, the switch $Q_1$and Q_4 are On , then $V_{prim} = V_{in}$ .In the second half the period $\frac{T_s}{2}$ to T_s switch $Q_2$and Q_3 are turned on and at time $V_{prim} = -V_{in}$. Similarly, in secondary side phase shift will be added therefore, at time $\frac{T_s}{2} + \varphi$, the switch Q_5 and Q_8 are On and in the second half period from $\frac{T_s}{2} + \varphi$ to $T_s + \varphi$ the switch Q_6 and Q_7 are On. Based

on the switching operation, the voltage in the primary and secondary sides of the transformer, inductor current, and voltage waveform are shown in Figure 3.6 when the converter is in operation.

The voltage across the inductor is the difference between the primary and secondary transformer voltage. Using the above inductor voltage, it is possible to find the current through the inductor, as shown in Figure 3.6 above. The inductor current I_L is in a trapezoidal shape in every half-cycle, and the average current through the inductor is zero. As previously mentioned, the secondary side active bridge works as a rectifier; therefore, the output current will be the rectified version of the inductor current. The rectified version of the inductor current is shown in Figure 3.7 below.

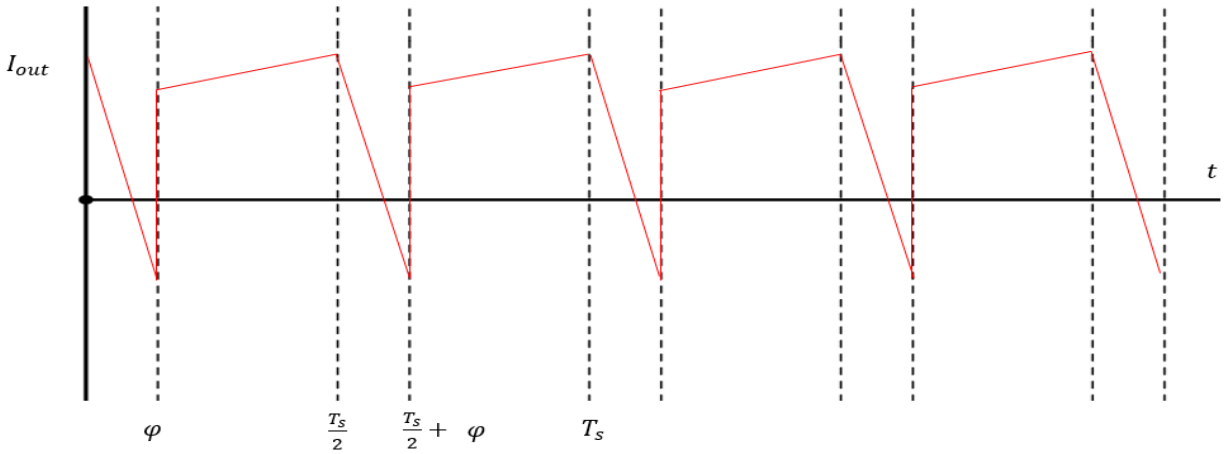


Figure 3.7. Output current or rectified version of inductor current.

The average output current is integral over – half the waveform cycle, which gives equation (3.8) below.

$$I_{out} = \frac{V_{prim}}{2 \cdot n\, L \cdot f_{sw}} D(1 - D) \;\; where\; D = \frac{\varphi}{T_s/2} \;\; and \;\; (-0.5 \leq D \leq 0.5) \qquad (3.8)$$

Similarly, output power can be found using output current and voltage, as shown in equation (3.9).

$$P_{out} = \frac{V_{sec} \cdot V_{prim}}{2\, n \cdot L \cdot f_{sw}} D(1 - D) \tag{3.9}$$

The above expression is the relationship between output power and the function of the duty cycle between the primary side and secondary side bridges, leakage inductance (energy transfer inductance), and switching frequency of the converter. On the other hand, a negative duty cycle or phase shift can cause inverse power flow from the secondary side to the primary side.

3.4 Power Losses

The power losses in a dual-active bridge are the unwanted energy losses that dissipate in the circuit during operating conditions. Several categories of losses are associated with designing a dual-active bridge: conduction losses, switching losses, and magnetic losses. The losses are the main reason for generating heat, and if components are temperature-sensitive, they can break down, causing the converter's efficiency to descend rapidly.

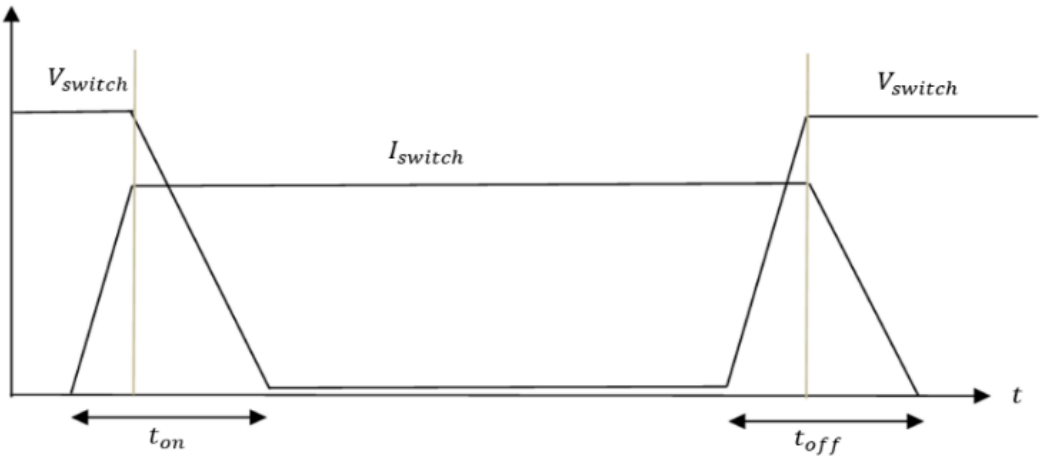


Figure 3.8. waveforms of switch turn-on and turn-off transient states

The switching losses appear in all eight transistors that transition from one state to another when they turn on and off [13]. Thus, the losses are based on the type of semiconductor device

used in the DAB converter. The switching implies the exposure of each transistor to voltage and current while dissipating power, or, in other words, the switching losses. Figure 3.8 shows waveforms of the power switches in the transient states. The switching losses in one transient state of one power MOSFET can be found using equation 3.10.

$$P_{switch} = \frac{1}{2} \cdot V_{switch} \cdot I_{switch} \cdot \left(t_{on} + t_{off}\right) \cdot f_{switch} \tag{3.10}$$

In the above equation 3.10 V_{switch} and I_{switch} is the voltage and current during the switching period and the time interval t_{on} and t_{off} are the turn-on and off time of the MOSFET and f_{switch} is the switching frequency at which the MOSFET operates. Note that high switching frequency is related to high switching losses.

Magnetic losses are the losses of the converter high-frequency transformer and series inductor. It is subcategorized into core losses and copper losses. The losses for the magnetizing current are very low and can be neglected. The series inductor is the magnetic part that can add to some losses. The core losses mainly occur due to the alternative magnetic flux in the core, hysteresis losses, and eddy current losses on the other side of those copper losses, also called winding losses. This is because of the losses due to the resistance of the copper winding of the primary and secondary winding of the transformer.

Conduction losses occur when the MOSFET is in continuous operation. They are the function of the RMS current in each bridge of the converter and the MOSFET's internal resistance.

3.5 High-Frequency Transformer and Leakage Inductance

As per the design requirement, high-frequency switching is employed, which reduces the size of passive components. At the same time, the magnetizing inductance becomes negligible at high frequencies. The transformer can be modeled only with a leakage inductor, representing the energy inductor of a dual active bridge. If the leakage inductance is insufficient to transfer energy, an inductor can be placed in series with the transformer. A high-frequency equivalent dual active bridge with a leakage inductor model is shown in Figure 3.9.

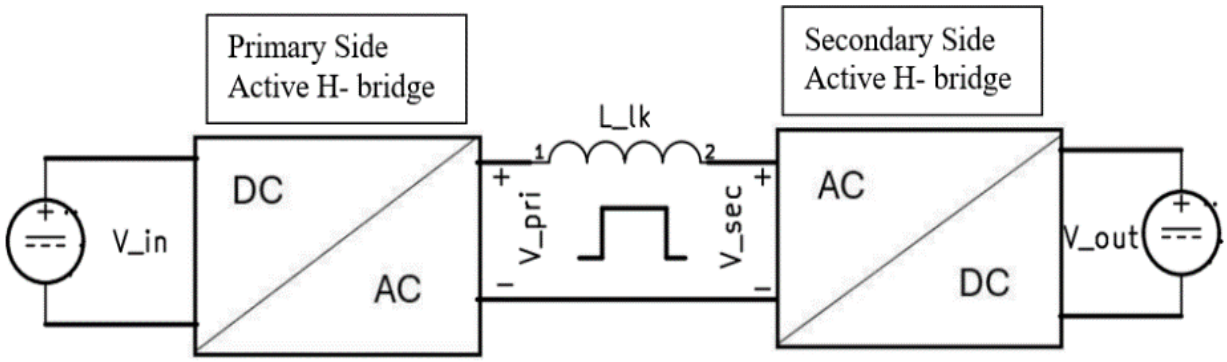


Figure 3.9. Equivalent dab model at high frequency

Figure 3.9 is an equivalent model of a dual active bridge in operating conditions, which consists of a primary side active H-bridge and a secondary side active H-bridge; the function of these bridges is to generate two complementary high-frequency AC square waves that can be phase-shifted with respect to each other. The generated AC square wave creates a voltage difference across this inductor—leakage inductance, which works as an energy transfer inductance. As per the power requirement, a high-frequency Payton Planar 6kW transformer with a turn ratio of n = 1.5 was used. Figure 3.10 shows the picture of the transformer used.

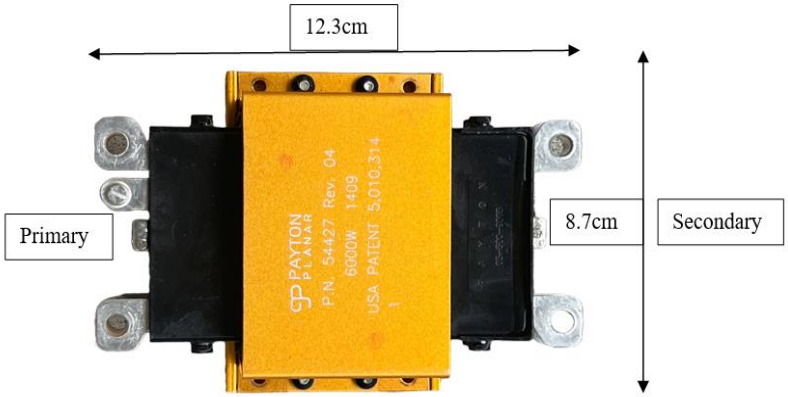


Figure 3.10. High-frequency Payton planar transformer

To measure the leakage inductance and magnetizing inductance, short circuit and open circuit tests have been performed using an LCR meter. Figure 3.11 various modes of measurement.

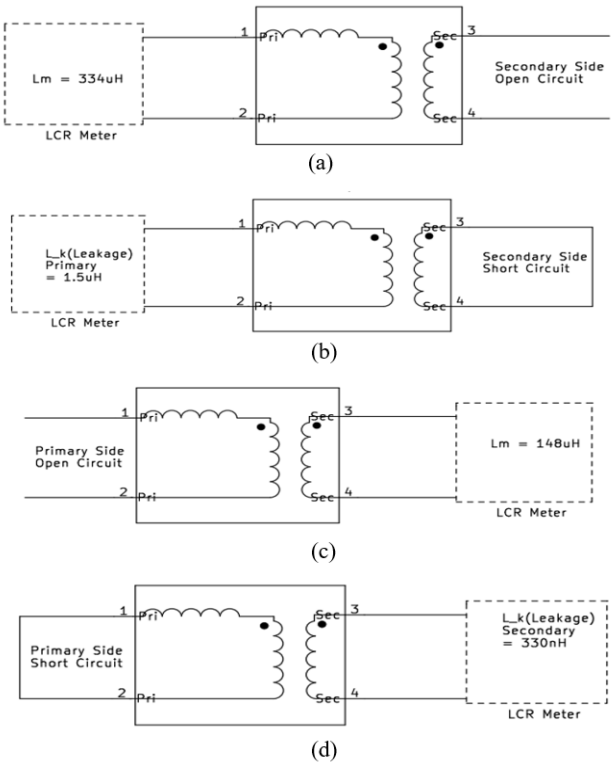


Figure 3.11. Short circuit and open circuit measurement using an LCR meter.

The model of the transformer can be understood by following the diagram below. Where R_pri and R_sec are the parasitic resistance, L_(lk_pri) and L_(lk_sec) are the respective leakage inductance, and L_m is magnetizing inductance.

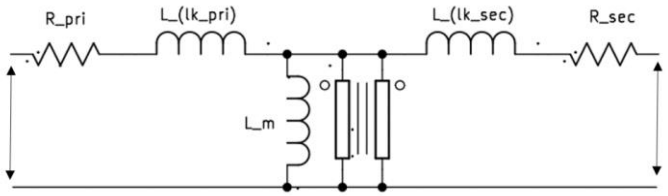


Figure 3.12: Model of transformer

For the sake of understanding, parasites can be ignored. The secondary side needs to be circuited to measure the magnetizing inductance of the primary side, as shown in Figure 3.11 (a). In that case, most of the power transfers through the Lm as it is huge compared to leakage inductance, and it became dominant in the path of current shown in the figure below in this Lm found 334 uH.

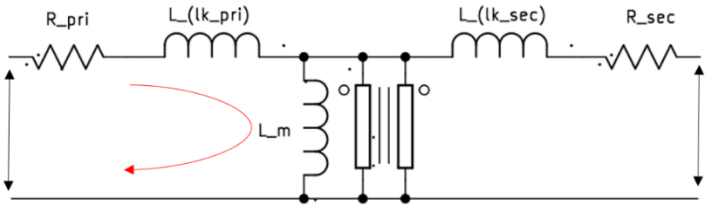


Figure 3.13: Current loop in transformer when secondary side open circuited.

On the other hand, the secondary side needs to be short-circuited to measure the primary side leakage inductance, as shown in Figure 3.11 (b). Then, most current passed through flowing L_(lk_sec) and R_sec as this path's impedance is low compared to Lm. In this case, L_(lk_sec) is known as leakage of the secondary, referring to the primary. Similarly, R_sec is known as parasitic resistance of the secondary referring to the primary. The path of the current is shown in the figure below, and the leakage inductance was found to be 1.5uH.

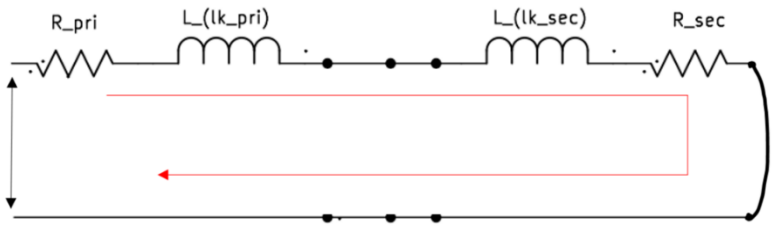


Figure 3.14: Current loop in transformer when secondary side short-circuited.

Similarly, the same procedure is used to find the secondary side's magnetizing inductance and leakage inductance, as shown in Figure 3.11 (c) and (d). The primary side's magnetizing inductance is 148uH, and the leakage inductance is 330nH. On the other hand, the turn ratio was found to be 1.5 using the equation (3.11) below.

$$n = \frac{N_p}{N_s} = \sqrt{\frac{L_p}{L_s}} = \sqrt{\frac{335}{149}} = 1.5 \qquad (3.11)$$

To determine the transformer's functionalities and parameters, a Keysight E5061B network analyzer was used, and the following result was measured.

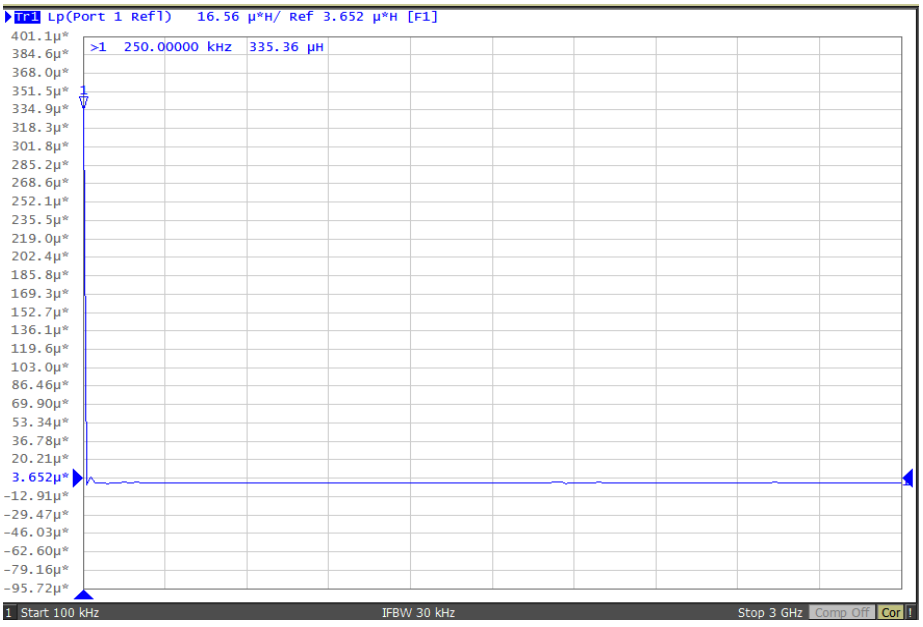


Figure 3.15: Primary side magnetizing inductance.

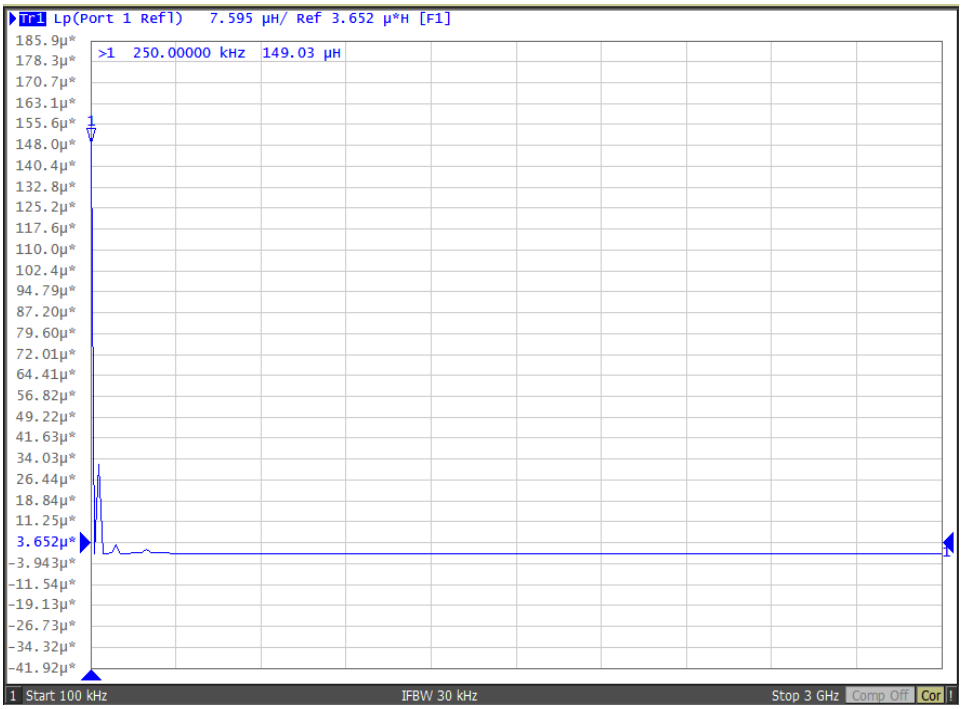


Figure 3.16: Secondary side magnetizing inductance.

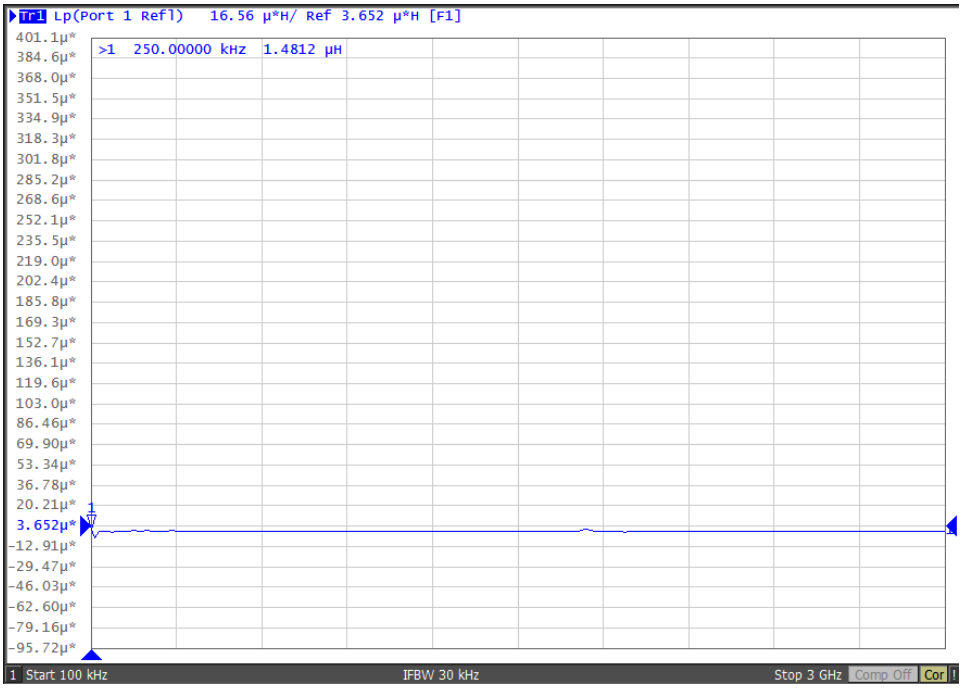


Figure 3.17: Primary side leakage inductance.

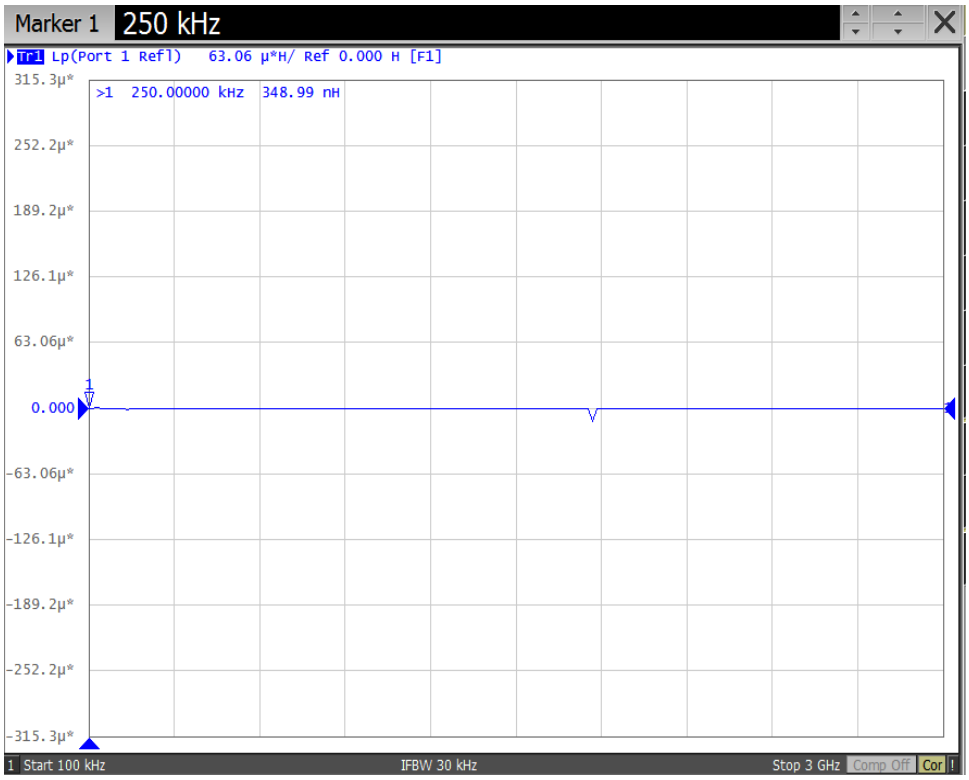


Figure 3.18: Secondary side leakage inductance

A MATLAB Script was written to find all the parameters shown in APPENDIX [A] and analyze the above data. The results of the MATLAB scripts are shown in the table below.

Parameter	Value (uH)
Magnetizing Inductance (Lm)	334
Turns ratio (n)	1.502251
Leakage reflected secondary to primary	0.000334
Leakage reflected primary to secondary	0.000754
Total leakage Inductance on the Primary Side	1.500334
Total leakage Inductance on the Secondary Side	0.330754

Table 3.2 MATLAB result of transformer's parameter

Equation 3.12 is used to find the required leakage inductance, which is a rearrangement of equation 3.9, as shown below. For the proposed converter, 6.6 uH was found.

$$L_k = \frac{\cdot V_{sec} \cdot V_{prim}}{2 \cdot n \, P_{out} \cdot f_{sw}} D(1 - D) \quad = 6.6\text{uH} \tag{3.12}$$

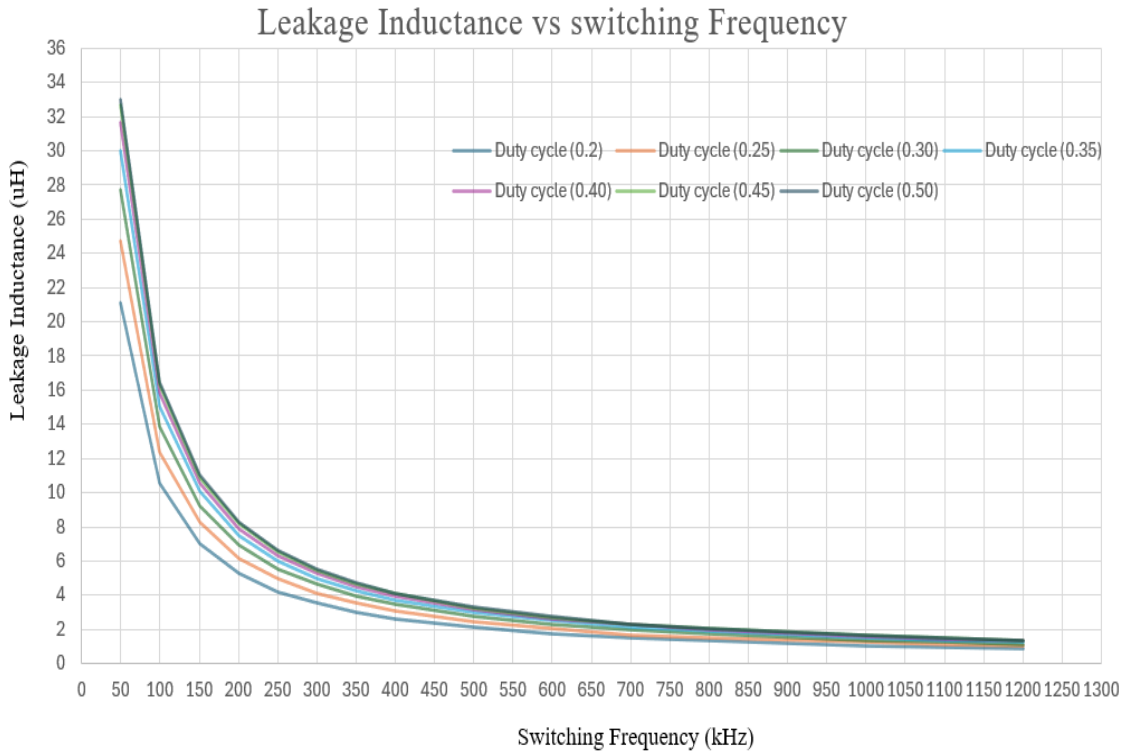

Leakage Inductance vs switching Frequency
Leakage Inductance (uH)
Switching Frequency (kHz)
Duty cycle (0.2)
Duty cycle (0.25)
Duty cycle (0.30)
Duty cycle (0.35)
Duty cycle (0.40)
Duty cycle (0.45)
Duty cycle (0.50)
0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36
0 50 100 150 200 250 300 350 400 450 500 550 600 650 700 750 800 850 900 950 1000 1050 1100 1150 1200 1250 1300

Figure 3.19 Variation of leakage inductance with switching frequency and duty cycle.

The above figure shows the relation between switching frequency and leakage inductance at different duty cycles for the required power transfer of the designed converter as per equation 3.12. It shows increasing switching frequency dramatically reduces the leakage inductance, and, at the same time, the low value of the duty cycle requires a low value of leakage inductance. On the other hand, the duty cycle does not have much effect when the switching frequency is very high. But at the same time, high frequency leads to high switching losses. Generally, the duty cycle is

placed between 30% and 40%, where maximum power can be achieved [14]. There are various factors involved in choosing a duty cycle. One of them is that the power transfer characteristic of the DAB remains mostly linear when the duty cycle is between 30% and 45%, allowing for better control and regulation of the power flow.

The measured value of leakage inductance of the Transformer is shown in Table 3.2. The Transformer chosen for this converter offers 1.5 uH leakage inductance, which is insufficient to transfer energy from primary to secondary at 250kHz. As per the above graph, the required switching frequency lies at more than 1Mhz to transfer desired power at leakage inductance near 1.5uH, but the Transformer gets saturated when the switching frequency goes higher than 500kHz. The primary reason is the transformer core gets saturated. Transformer saturation occurs when the core material reaches its magnetic flux density limit and can no longer efficiently store magnetic energy. On the other hand, ringing was observed on the primary and secondary sides of the Transformer. The main reason for ringing can be low leakage inductance. [15], which resonates with the parasitic capacitance of the designed module, forms an LC circuit, and generates voltage spikes, as shown in the figure below. Therefore, adding a series inductance has two benefits: one, it adds up with leakage inductance, acts as energy transfer inductance, and allows an operating frequency near 250kHz, and two additional inductors significantly reduce the ringing shown in the figure below. The frequency of ringing can be calculated using the equation (3.13) where L_k is leakage inductance and C_p is parasitic capacitance; therefore, the series inductor adds up with leakage inductance and lowers the ringing frequency.

$$F_{\text{ring}} = \frac{1}{2\pi\sqrt{L_k * C_p}} \tag{3.13}$$

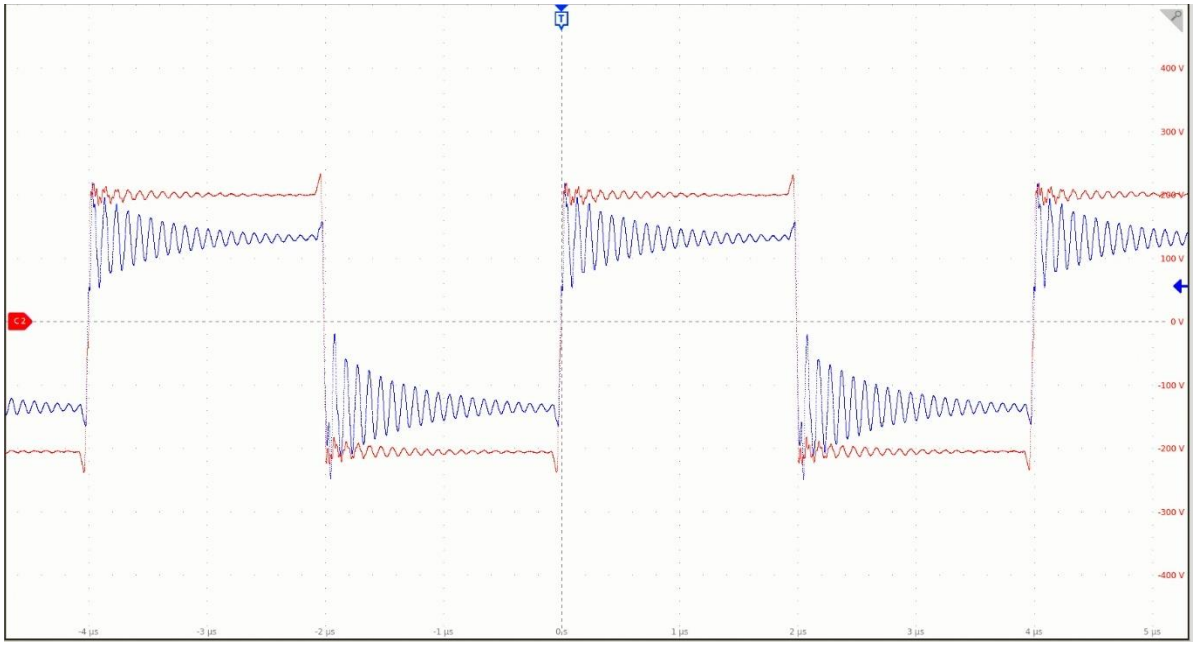


Figure 3.21. AC voltage waveform in the primary and secondary sides of the transformer with ringing (no inductor)

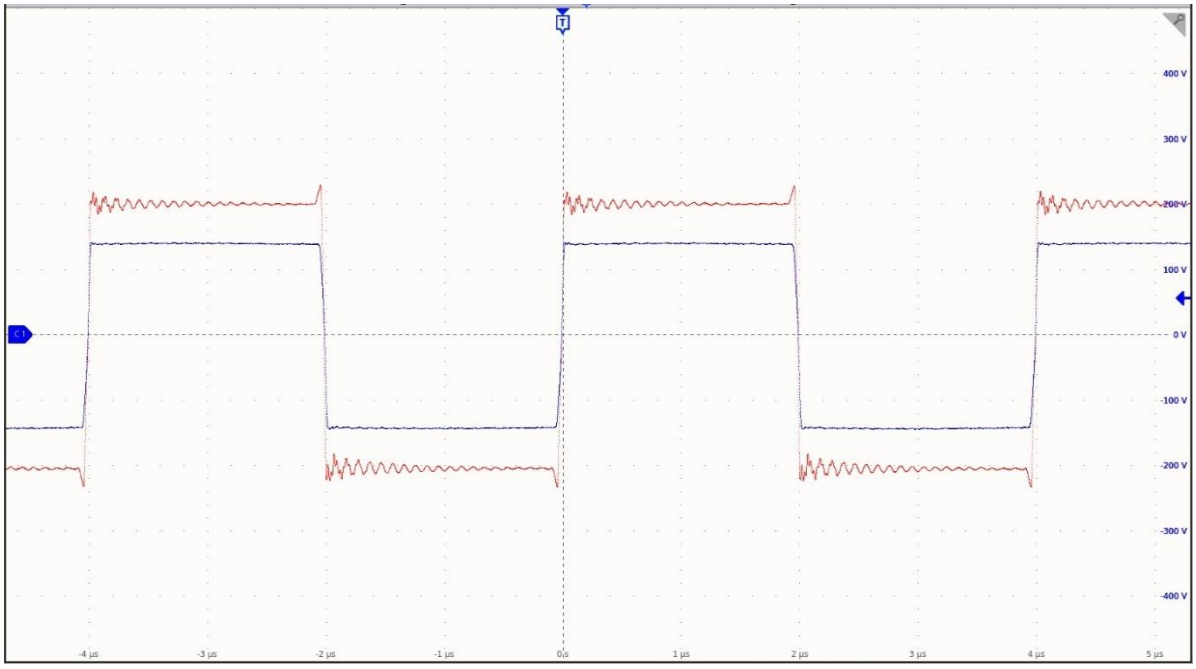


Figure 3.22. AC voltage waveform in the primary and secondary sides of the transformer with less ringing (with energy inductor)

3.6. Zero Voltage Switching.

The concept of Zero-Voltage Switching (ZVS) has been introduced previously. It is a natural capacity for soft switching in the form of ZVS. Concerning a DAB converter, ZVS occurs when “the switches (usually MOSFET or IGBT) operate while the voltage across them is approximately equal to zero.” To this end, the switches transition from their conducting to non-conducting phases and vice versa when the voltage across them is almost zero. As such, the ZVS helps to minimize switching losses associated with switching the switches on and off.

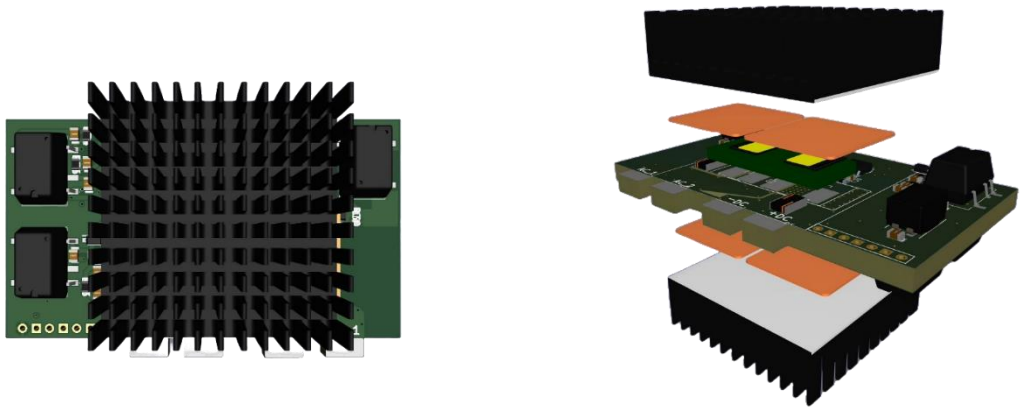
The ZVS allows the converter to switch softly and decreases power losses at high frequencies. [16]. As equation 3.10 shows above, high switching frequency is a major reason for switching losses. The dead time of the switching frequency plays a critical role in achieving ZVS. During dead time, the power MOSFET of the active full bridge is off, for instance, but the inductor current needs to continuously flow through the body diode MOSFET of SiC or the opposite direction in GaN switches (Due to its reverse conduction ability) [11] As the inductive current is AC, it can naturally choose its path of flowing where low blocking voltage or nearly zero. The blocking voltage of this anti-parallel diode or reverse conduction of GaN is much smaller than the blocking voltage of MOSFET. Therefore, achieving ZVS by introducing dead time is a more effective way to lower the switching losses. On the other hand, zero current switching (ZCS) is achieved through control and, therefore, prevents the use of phase-shift modulation, while ZVS is achieved through topology.

CHAPTER 4

650V / 60A GaN BASED POWER MODULE DESIGN

4.1 Introduction

After considering the above charger specifications, the converter must have a 450V maximum voltage and a 22 A current to achieve the required power rating. Using the characterization of the output voltage derivative of a quadrature voltage loop and differentiation of a quadrature current loop, a GaN (GS66516T) -based full bridge module containing the gate driver and isolated auxiliary power supply was developed. The design of the GaN module has highly optimized electrical features, including a compact design and much shorter power and gate driver loops. Its packaging and printed circuit board design have optimized electrical properties, including low gate inductances and commutation loop inductance, thereby minimizing switching losses to high-speed rapid switching. On the other hand, from the perspective of its high voltage and current operation, an electrical design is still made for this aspect, which must ensure safety. The thermomechanical design concept of the GaN module involves faster heat transfer from the GaN switch junction to the heatsink. The 3D concept design is shown in Figure 4.1 below.



(a) 3D model of the designed module (b) Exploded View of the developed module.

Figure 4.1: 3D Design of GaN-based full bridge power module.

4.2 Design concept

The power module is designed to ensure a minimized commutation loop, and PCB traces are chosen in such a way that current flows in opposite directions to each other in PCB traces, which cancels the mutual flux and achieves low power loop inductance. Therefore, a double-sided flip-chip structure is used to mount GaN devices on a PCB, which also gives additional advantages of double-sided cooling to the power module. The problem with such a structure is that the height of the GaN devices (GS66516T), the height of the decoupling capacitor, and the gate driver (SI8271) used in the module are mismatched, and this is leading to a mounting issue. To solve this issue. [2] Two PCB spacers on the daughter board are used, as shown in Figure 4.2, which solves this height mismatch issue and provides room for passive components.

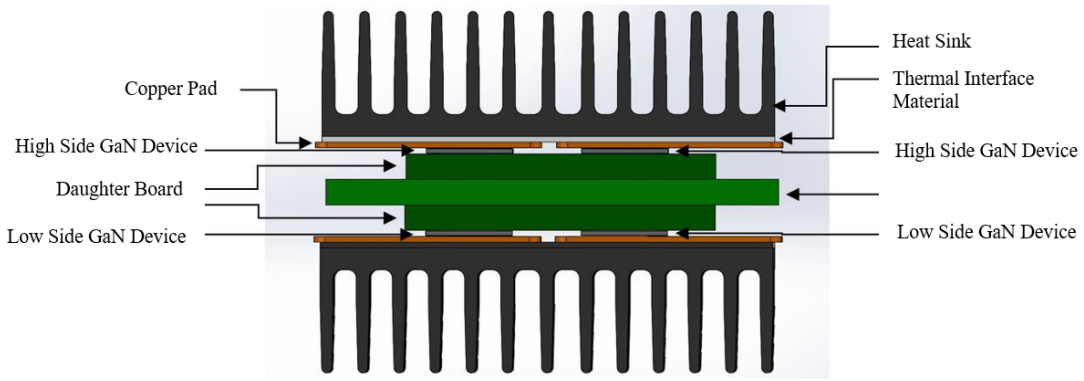


Figure 4.2. Side view of CAD file of the designed module

The power loop and gate loop are routed inside the motherboard PCB. The GaN Devices GS66516T provides a top-side cooling thermal pad, which can be directly used to solder with an additional copper pad to maximize the heat flow and improve the rigidity of the module, as shown in Figure 4.2. This copper pad provides a wide area of heat flow to the heat sink. The copper pad is glued with a heat sink and glued with a thermal interface material tap (3M thermally conductive adhesive transfer tapes 8805), which has 0.60 (W/m-K) thermal conductivity. On the other hand, the copper pad chooses an optimized area as connected to the thermal pad of GaN devices, which

is internally connected to the source potential (AC) of high-side GaN devices; when it is glued with the heatsink, it works as a parallel plate capacitor or stray capacitance and thermal interface material act as a dielectric material. When the device operates at high frequencies with high current and voltage, this stray capacitance can lead to EMI issues, and therefore, it is recommended to ground the heat sink.

4.3. PCB schematic and layout design

Due to EMI and crosstalk issues, PCB layout design becomes very challenging when the circuit operates at high frequency. Therefore, it is very crucial to know the switching behavior of the GaN switch and gate driver circuit at high frequencies. Designing a gate driver circuit for fast-switching devices requires various considerations, such as the type of isolation and level of isolation. The gate driver should be capable of providing turn on and turn off voltage and current as per the requirement of gate-source saturation region or ohmic region power MOSFET, should be able to do level shifting, acceptable propagation delay, should have low parasitic, low isolation capacitance, high impedance in the input side, sufficient level of standard mode transient immunity (CMTI). On the other hand, GaN devices have high dv/dt and di/dt during the transition period [3]. The primary reason for this is that it has inherent fast switching speeds and low parasitic capacitance compared to silicon devices. GaN devices have low input capacitance (Ciss), which allows fast-changing and discharging of the gate in the switching period and leads to high dv/dt. The threshold voltage of GaN devices is low; therefore, a slight change in gate voltage causes a more significant change in drain current and spikes the high di/dt. Due to these high transients, gating GaN devices becomes more challenging; therefore, careful gate driver design and optimized layout design are needed. At high frequencies, the miller capacitance or Cgd (Capacitance between gate and drain) provides a leakage path, which can lead to crosstalk between the power loop and gate loop and, at the same time,

parasitic due to high frequency can make it more effective and contributes to switching losses. The topologies used to design power modules are either half-bridge or full-bridge configurations, and power devices are turned on and off in a complementary fashion. When the bottom switch is turned on then, a positive gradient of dv/dt forms across the top side switch and induces a displacement current through the miller capacitance, and it needs to sink to the gate driver IC if the return path of this displacement current passes through the turn-on gate resistor and this positive voltage spike higher than the threshold voltage, this could lead to unwanted losses and may damage the devices; therefore, a separate path needs to provide. Similarly, when top devices are turned off, a negative gradient of dv/dt forms across the bottom side switch and again induces a displacement current but in the negative direction if this current passes through the turn-on gate resistor of the bottom side switch and induces negative voltage spike higher than the threshold voltage, this could again lead to unwanted losses and may damage the devices. Therefore, the gate driver needs two different paths with different gate resistance to mitigate this problem, and gate resistance needs to be chosen carefully as it controls the switching speed of the device. Considering the above challenges in designing a gate driver circuit for GaN devices, component selection, and layout design have become very selective. The gate driver Si8271 from Silicon Lab was selected, which provides a separate path to flow turn-on and off current, or, in other words, two separate source and sink pins. It comes with a buffer and an isolator inside the package. It provides 200kV/μs CMTI, 2.5kV RMS voltage isolation, and very low primary-secondary stray capacitance (0.5 pF). Figure 4.3 below shows the schematics of all four-gate driver circuits for high-side and low-side devices. Note in the high side gate driver circuit (top left figure) that R19 is a turn-on gate resistor, which is 10 ohms. This value can be adjusted to achieve the desired slew rate.

Similarly, R23 (1 ohm) is a slightly smaller turn-off gate resistor, so the reverse gate current can pass through this path.

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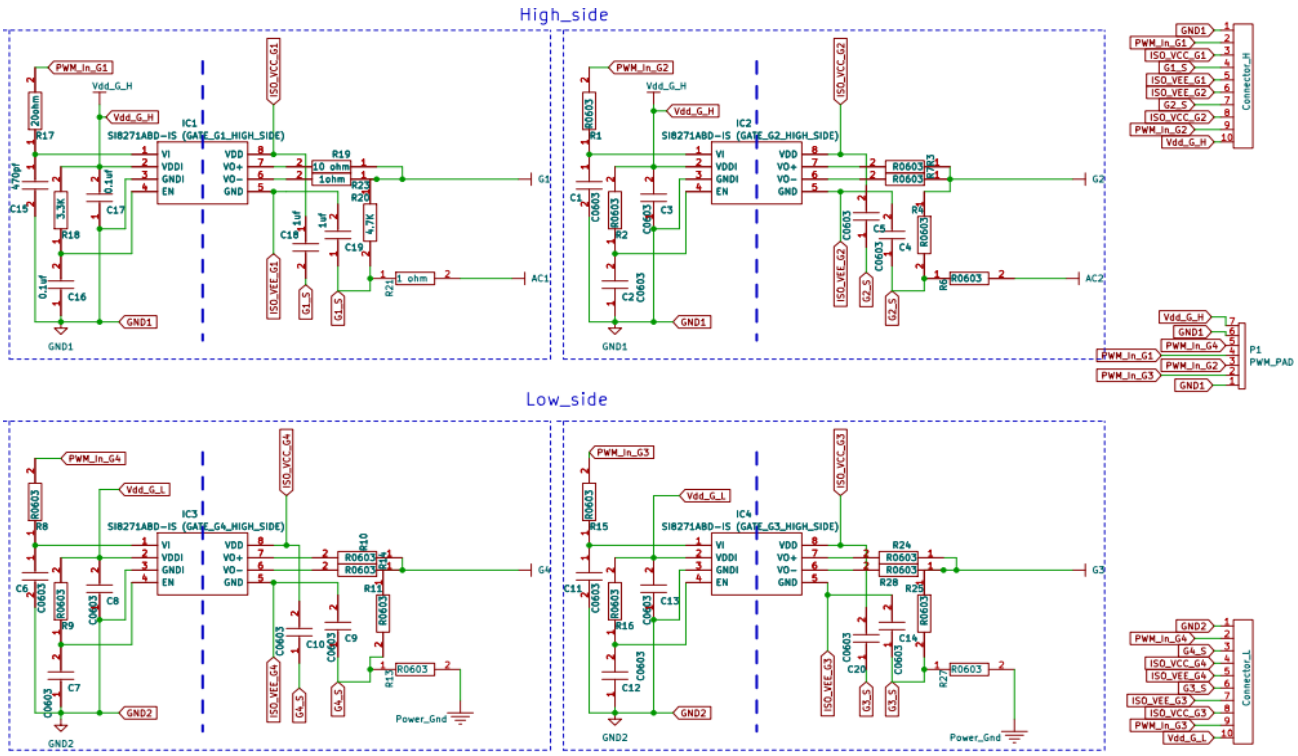


Figure 4.3. Schematics of gate driver circuit design

For GS66516T, the recommended gate driver voltage range Vgs is 0V to +6V. GaN systems devices do not require negative gate voltage to turn off, but for a safe operation against the voltage spike on the gate side of devices, typically, Vgs = -3V is used. To fulfill the requirement, isolated auxiliary power supplies have been designed. To design the power supply, CUI Inc's SMD 1 watt and 1kv Isolated Module DC-DC Converter was used where the output voltage is 9V and the input voltage is 4.5V - 5.5V. Further, this 9V output voltage is split into +6V and -3V using a diode and resistor, and the midpoint is used as ground 0V, and it should be connected to the kelvin source or source pin of GaN devices.

For better noise immunity, an SMD Common Mode Choke is used. Figure 4.4 shows a schematic of the auxiliary power supply design. At high frequencies, the behavior of passive components also changes. [17]. A resistor acts as a series combination of inductances, a capacitor acts as a combination inductor series on both sides with resistors, and at high frequencies, an inductor and capacitor change their impedances due to these parasites. Similarly, at high frequencies, when current travels through the transmission line or PCB traces, time-varying electric and magnetic fields are developed; therefore, RF energy comes into play, and that is the main reason EMI in the high-speed circuit, to minimize the effect of parasitic and EMI routing in the PCB need to be done very carefully.

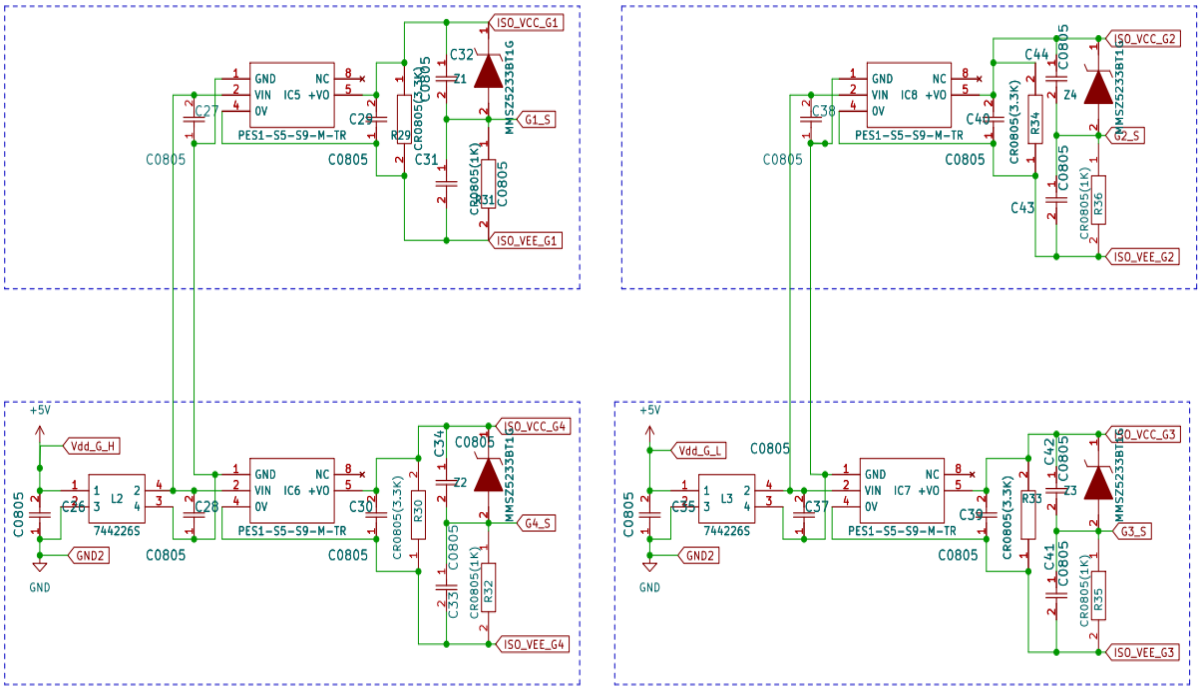


Figure 4.4. Schematics design of auxiliary power supply

The routing of the return path traces adjacent to each other or parallel to each other offers low loop inductance. Similarly, in the case of gate driver circuit design, to minimize loop inductance, the gate driver should be placed as close as possible to GaN devices. Lowering the loop inductance

using wide PCB traces and polygons can be very helpful. On the other hand, the power loop is routed within multiple layers with optimized thickness and width with vias, where vias play a curtail role in the layout for power distribution. Placement of these visas minimizes loop inductance and resistance and improves the overall performance of the circuit as it helps equally current distribution across the power trances, reduces the heat flow, and improves the overall reliability of the module. PCB design is shown in Figure 4.5 below.

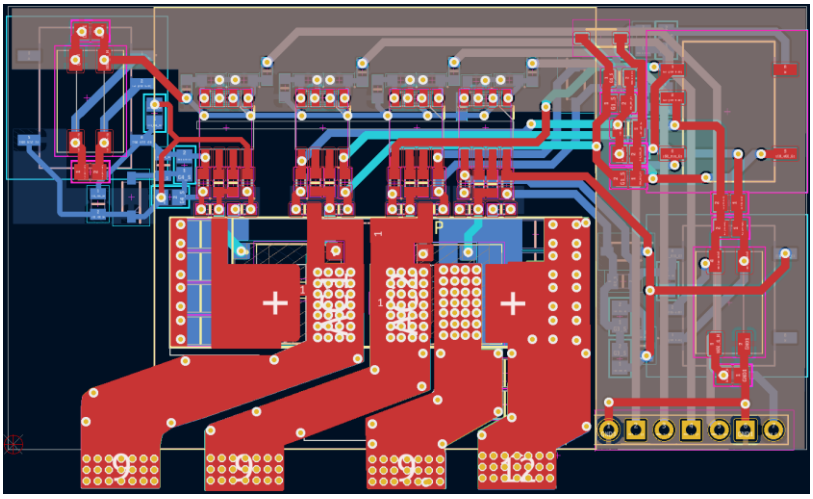


Figure 4.5 PCB design of the module

Multiple vias were used to lower the gate inductance, zoomed in in Figure 4.6, as shown below. The gate driver is placed as close as possible to GaN devices, and the PCB traces' return path is kept parallel to the gate signals to minimize loop inductance.

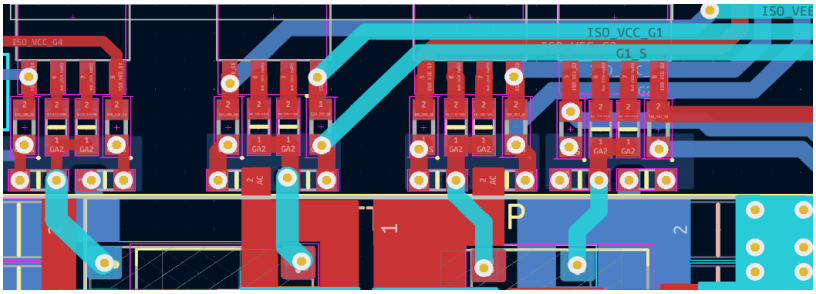


Figure 4.6: Zoomed view gate driver side of PCB design

Apart from the main board, two daughter boards have also been designed. As previously mentioned, the function of these daughterboards is to provide space and connection of +VDC and -VDC to a pair of switches, as shown in Figure 4.8. On the other hand, the connection of the H bridge is embedded inside these daughterboards. Figure 4.7 shows the schematic of the H bridge, where complementary GaN (GS66516T) switches are marked as pairs.

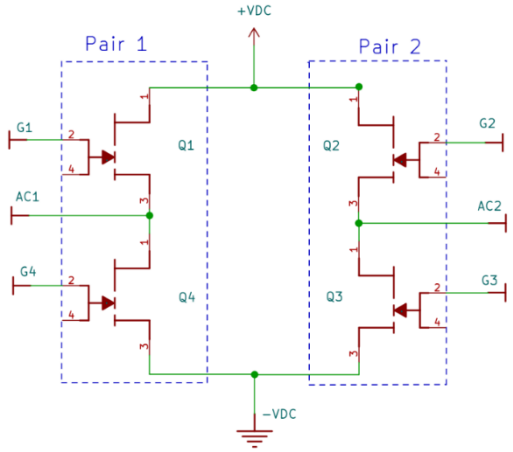


Figure 4.7. The schematic design of the H-bridge used in the module.

(a)PCB design of top side's daughter board (b) PCB design of bottom side's daughter board

Figure 4.8. PCB design of daughter board

The commutation and power loop can be understood from Figure 4.9, where Figure (a) shows the loop inductance and Figure (b) shows the Interconnection of the PCB layer.

(a) Loop Inductance (b) Loop Inductance

Figure 4.9 Loop communication

4.4.Assembly process of module

The power module is assembled using various reflow soldering. Initially, the components of the auxiliary power supply, gate driver, decoupling capacitor, and other passive components are attached to the main board. GaN chips are soldered with the daughterboard at the same time using SAC 305 solder paste. Finally, the copper pad, mainboard, and daughterboard are soldered together using solder paste. Figures 4.10 and 4.11 show the CAD file of the PCB design.

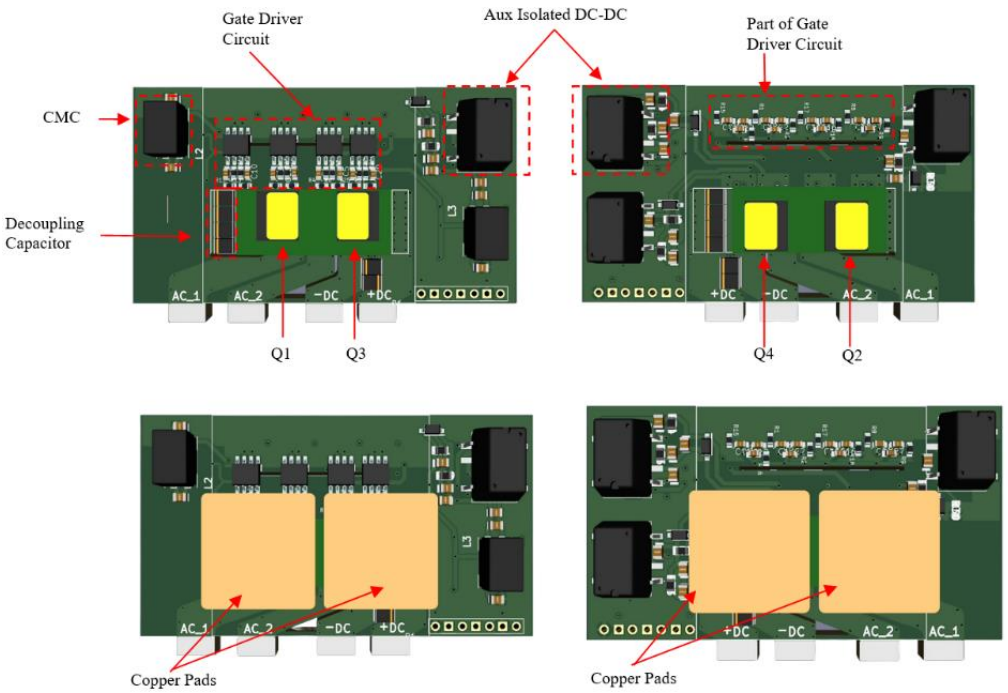


Figure 4.10 The figure CAD view of the Top and Bottom sides of the PCB design with a 3D step file of components.

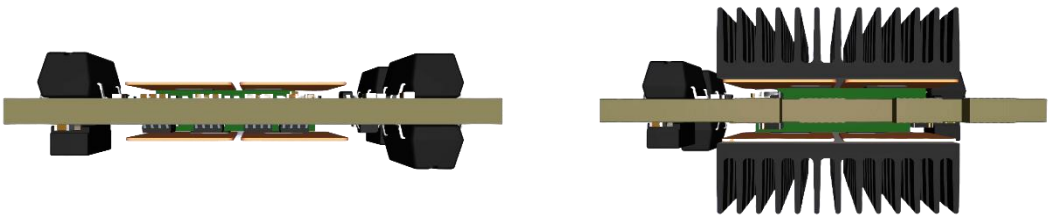
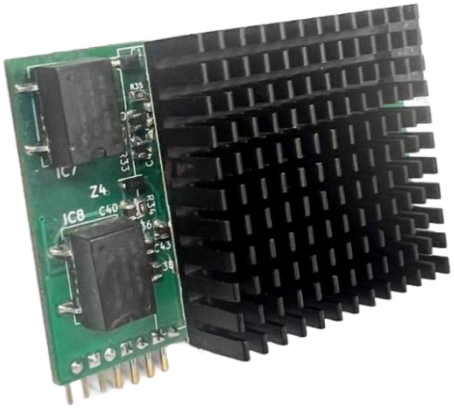


Figure 4.11 Side View of PCB CAD file with and without heat sink

Figure 4.12 below shows the actual picture of the assembled Module; the picture on the Left side is without a copper pad, and the right side has a copper pad, and Figure (c) shows the complete module with a heat sink.

a) Fabricated module without copper pad b) Fabricated module with copper pad



c) Complete Fabricated module with heatsink

Figure 4.12 Picture of fabricated module

4.5 Functioning Test and Double Pulse Test

To Check The functionality of the design board, the Texas Instruments LAUNCHXL-F280049C Development board was used, and a code was written in code composer studio to generate PWM signals. The PWM pin of the F280049C DSP board is shown in the figure below, and the C code is shown in APPENDIX[B].

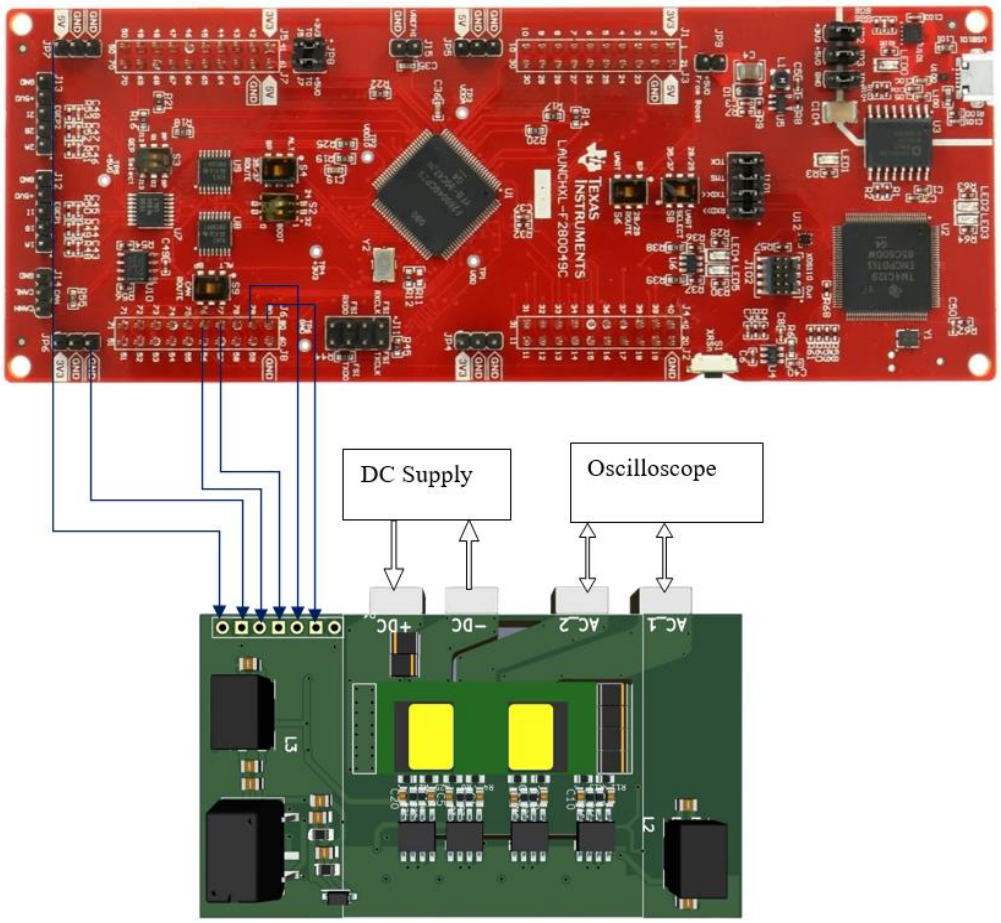


Figure 4.13 Functional testing setup of the module

The ePWM1 and ePWM2 pins are connected to the gate signals pin of the module, and the +5 and GND supply are also connected to the DSP board. On the other hand, another DC supply is connected to the +VDC and -VDC pins of the module and supplies 32V DC, and an oscilloscope is

connected to the AC1 and AC2 pins of the module to check the AC waveform. To test the function of the module, a 250kHz frequency pulse wave was applied using a DSP board. The output waveform is shown in Figure 4.14, where small ringing was observed due to parasites.

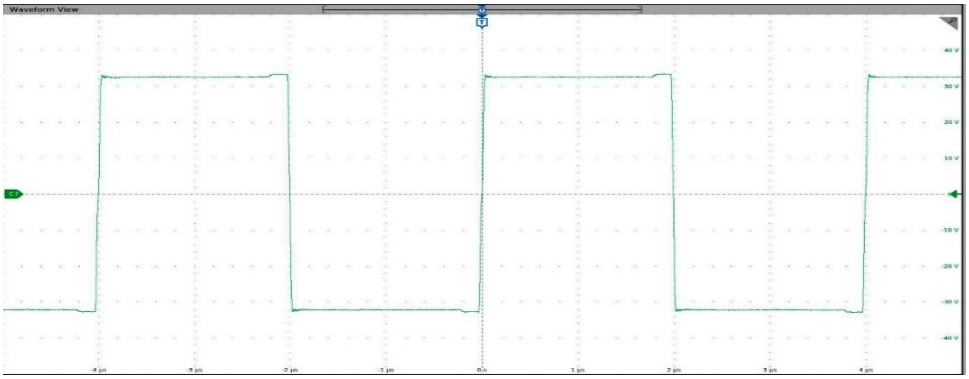


Figure 4.14 AC output waveform

A double pulse test was performed to determine the switching characteristics and performance. In the DPT setup, converter circuit conditions are replicated by introducing an inductive load. Power is supplied to the inductor to simulate operational conditions and facilitate the assessment of switching losses. The DPT test for the designed module was only conducted on the low side switch of the half-bridge. Figure 4.15 shows measurement points of the double pulse test for the low-side switch.

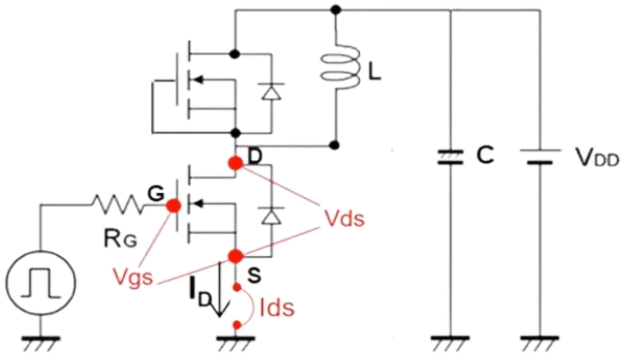


FIGURE 4.15 Double Pulse Test Measurement Point

The module is mounted on a secondary PCB holding a DC link Capacitor, as shown in the figure below. All measurement points are connected as per the above figure, and an air core inductor (1800uH) has been connected to the high side switch of one-half of the module's bridge. The other half of the bridge is kept turned off during the test. The module was tested up to 480V and 20A current, as shown in the figure.

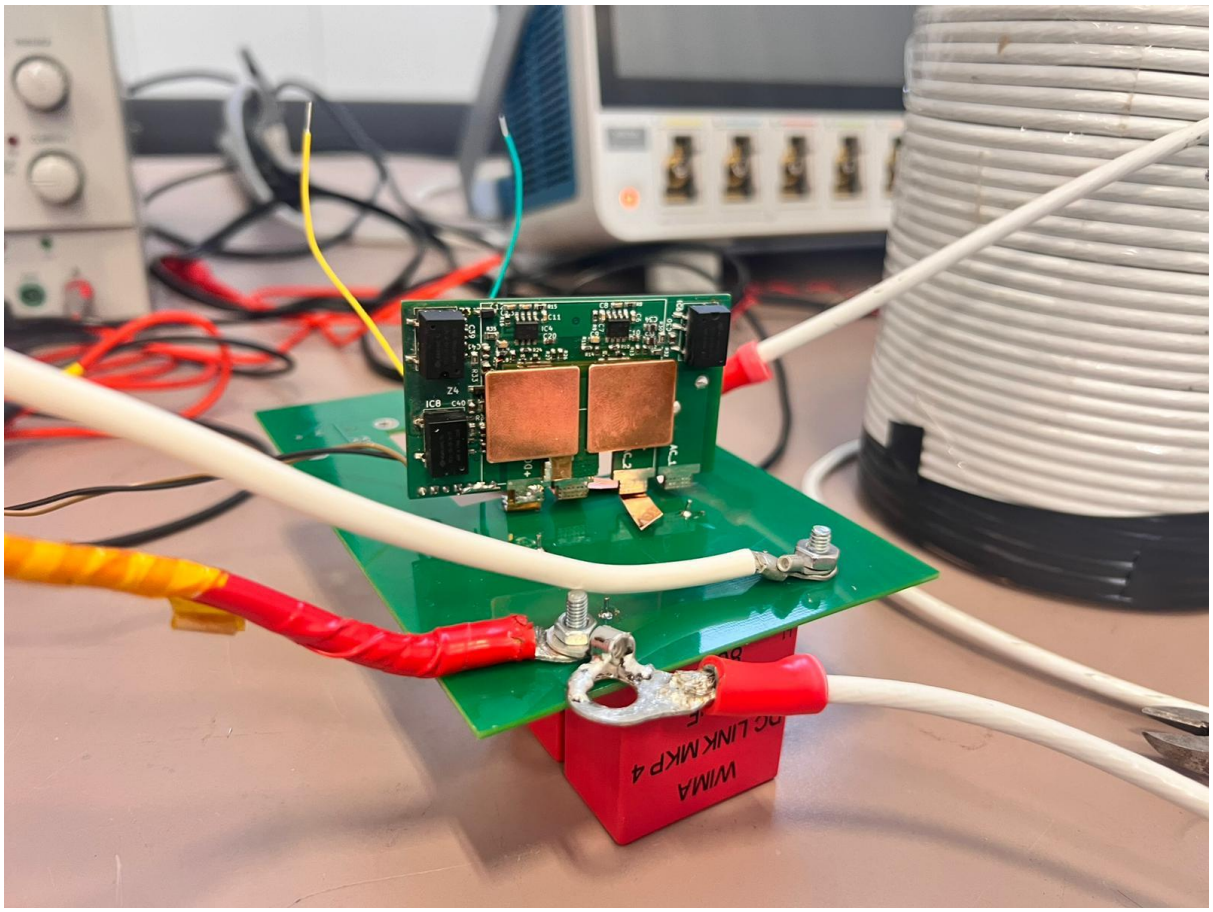


FIGURE 4.16 Double Pulse Test Setup

The figure below shows the low-frequency ringing in the drain current. One possible reason for the ringing was the interaction of the devices' high di/dt and parasitic inductance and capacitance, which were introduced due to PCB traces between bus bars and the power loop. On the other hand,

the parasitic inductance in the power loop may create a resonant circuit with GaN devices' output capacitances, known as Coss, resulting in low-frequency ringing or damped oscillations in the drain current [18].

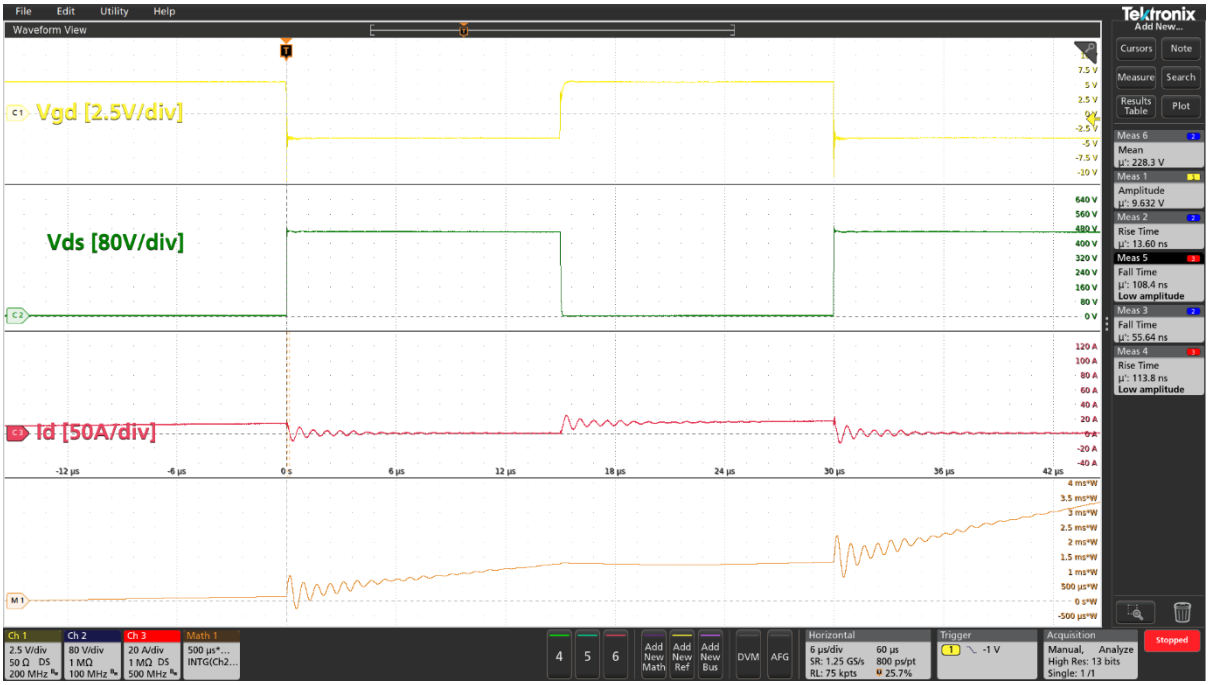


FIGURE 4.17 Result of Double Pulse Test

CHAPTER 5

DESIGN CONSIDERATION OF CONVERTER

5.1 Design Specifications of the Converter

Various design parameters need to be considered when designing the converter. Table 3.1 below shows the most fundamental specifications of the converter needed to design a level 2 EV charger.

Parameter	Value
Topology	Single-phase-shift, Dual Active Bridge
Power Module	Full-bridge GaN module (GS66516T, 650V, 60A) with Air cooling
Sensing	Isolated voltage and current sensing
Maximum Power Output	5 kW-6 kW
Primary Voltage	380-450 V DC
Secondary Voltage	230-260 V DC
PWM Switching Frequency	250 kHz with soft switching
Controller	TI TMS320F280049 DSP board
Maximum Output Current	27 A
Transformer	Payton Transformer (n = 1.5 with leakage 1.5 uH)

Table 5.1: System Specification of Converter.

The preliminary maximum output power is between 5kW and 6kW, and the output voltage is between 240 and 260 V. Therefore, the output load resistance can be found using the following equation.

$$R_{load} = \frac{V_{out(max)}^2}{P_{output}} = 12.5\ \Omega \text{ (for 250 V and 5kW power)} \quad (5.1)$$

The output voltage should be a pure DC voltage, but the voltage at the output side always

has some ripple due to an unbalance of electron charges at one switching period; therefore, it is essential to suppress this ripple within the tolerance range, ideally for constant DC output voltage a large value of capacitor needed, and practically impossible to manufacture such large capacitor because of size and also it will raise costs of the converter. Therefore, capacitor values need to be chosen to limit the ripple and lie in limited size. Typically, equation (5.2) is used to find the value of charge, and it can be derived using the output current waveform shown in Figure 3.6 [19]. The value of chosen D = 0.5 as peak energy can be obtained at the large output power. The value of the capacitor depends on the charge found and the ripple voltage allowed in output; therefore, equation (5.3) is used.

$$\Delta Q = \frac{n.V_{prim} \cdot D^2}{4 \cdot L \cdot f_{sw}^2}\left[(1-D) + \frac{D^2}{4}\right] \quad = \quad 0.00005113 \text{ C} \tag{5.2}$$

The ΔV_{out} ripple is considered as minimum as possible based on the availability of capacitors in the market, $2\Delta V_{\text{out}} = 0.165$ V

$$C_{\text{out}} = \frac{\Delta Q}{2\Delta V_{\text{out}}} \approx 310\ \mu\text{F} \tag{5.3}$$

Therefore, the near value of capacitor 330uF with an appropriate size was found for the output side. Similarly, the input side capacitor found 195 uF, and the nearest value used was 220 uF.

5.2 Simulation of the proposed converter design

The converter simulation was performed on the PLECS standalone. The software was the best choice for the high-frequency design. It provides advanced tools for simulating the dynamic complex

power electronic system. Some advanced features characterize the PLECS software, such as the silicon carbide and gallium nitride devices. The simulation process followed two main steps, as shown in Figure 5.1. Firstly, it was a controller design shown in Figure 5.3. Guidelines and practice for control algorithms and feedback loops were developed, and the simulation ensured that the converter worked at the best performance and had the appropriate specifications. Following the controller design, the converter design shown in Figure 5.2 was also simulated, and the partial power electronic system was evaluated. The simulation determined the complete system performance, including the controllers' performance, the switching devices' behavior, the passive components, and the chosen load. Simulation in two stages allows for conducting simplified optimization of the designed system. The control design ensures the robust performance of the control strategy. In contrast, the system design stage defines the performance quality of the designed power electronic system under load and operation changes. PLECS also uses simulation parameters known as model initiation commands APPENDIX[C], which show those commands in text format.

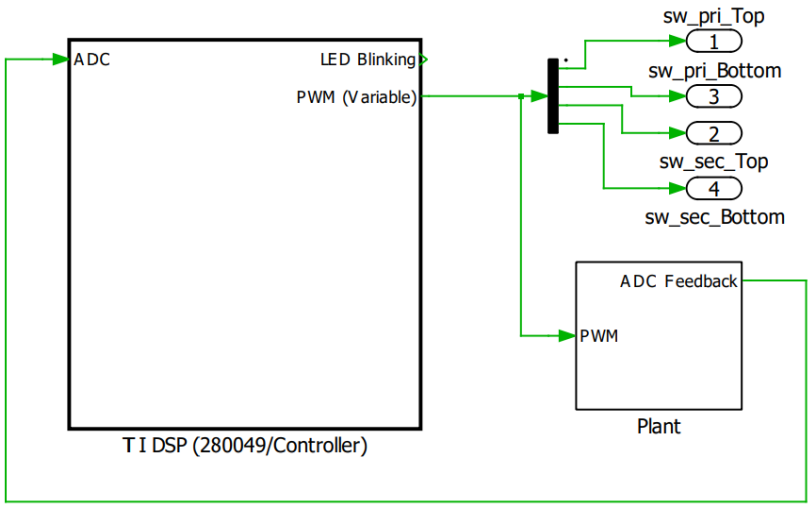


Figure 5.1. The first page of the simulation

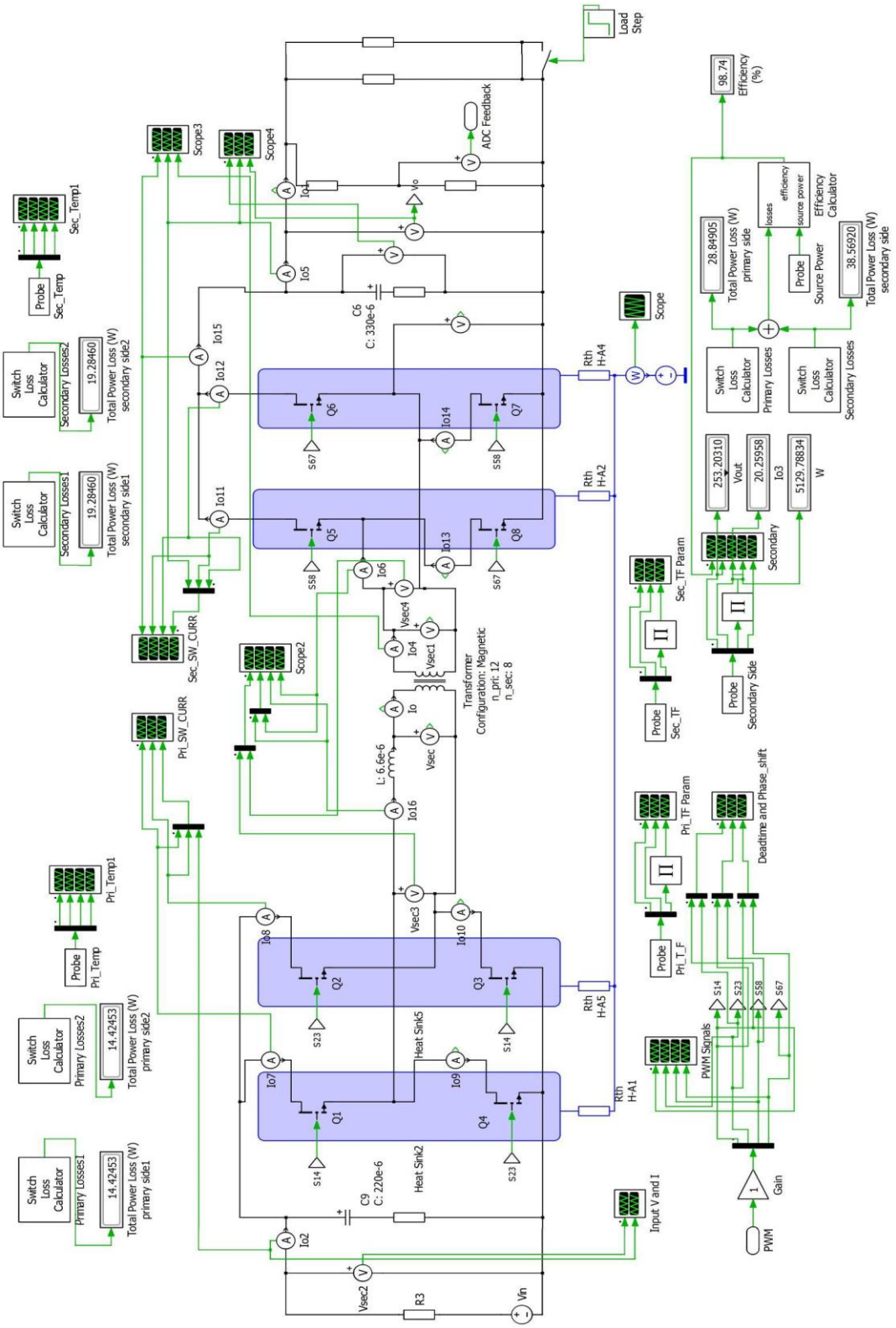


Figure 5.2. Second page of simulation (simulation of converter design)

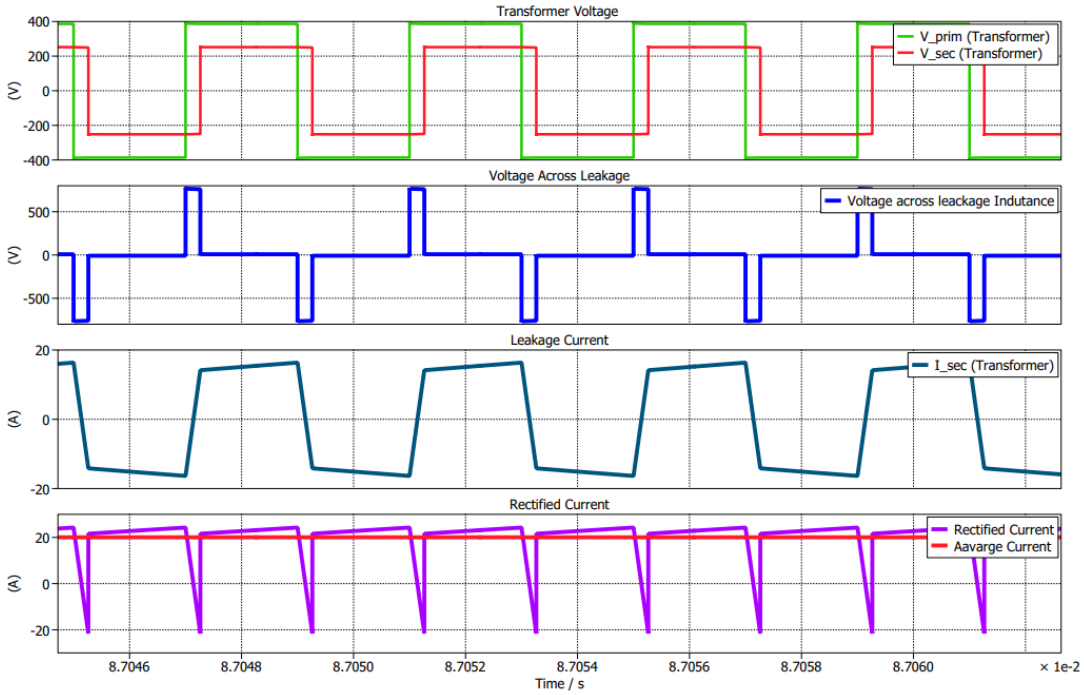


Figure 5.3 Simulation result 1 (transformer voltage, leakage current, and voltage waveforms)

Figure 5.3 shows the voltage across the transformer, the voltage across the leakage inductance, the current waveform across the leakage inductance, and the rectified current waveform.

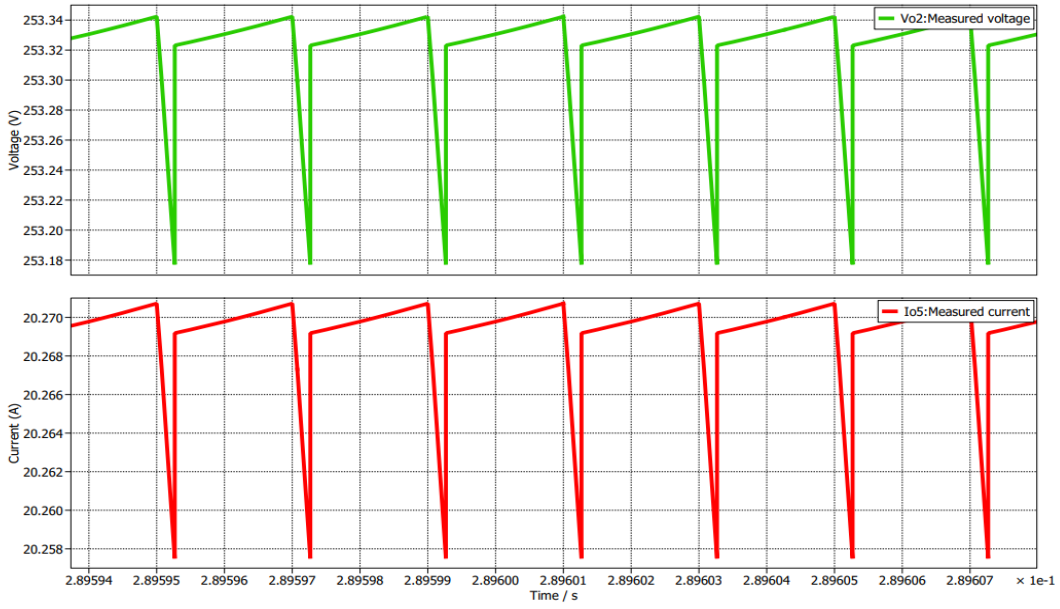


Figure 5.4 Simulation result 2 (rectified voltage and current waveforms)

Figure 5.4 shows the rectified voltage and current waveform. This waveform needs to be filtered out before being applied to a load. Here, a DC link capacitor suppresses the ripple in the voltage waveform.

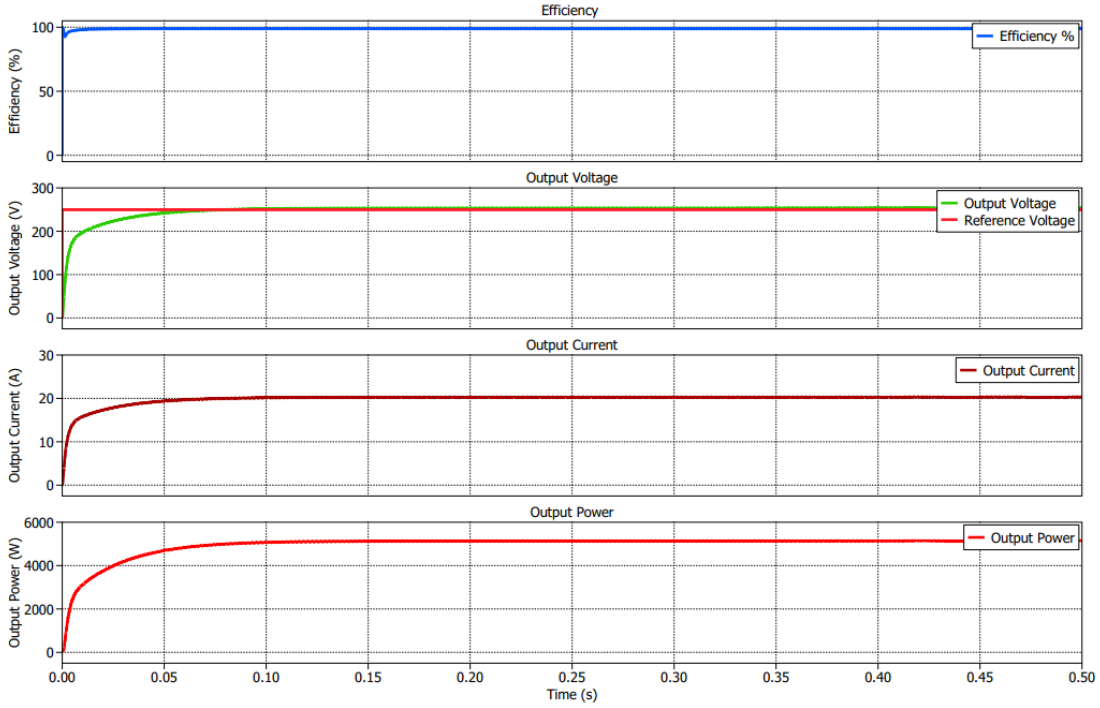


Figure 5.5. Simulation results 3 (Output Voltage, Current, Power, and Efficiency Waveform)

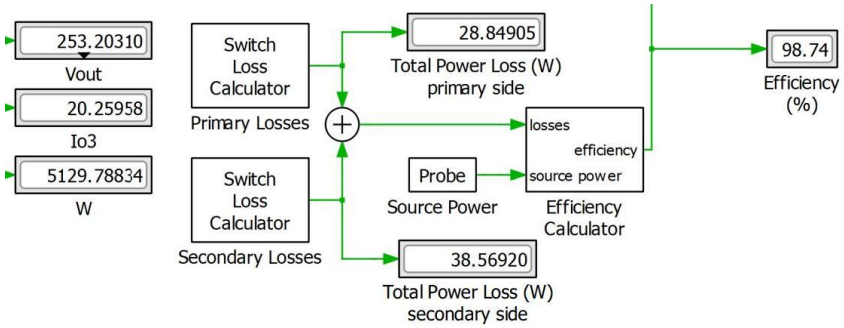


Figure 5.6 Efficiency calculator using PLCES simulation.

Figure 5.5 shows the output voltage, current, output power, and efficiency waveform; the output voltage comes to 253 V, the output current is 20 A, and the output power is 5129 watts with 98.74 % efficiency.

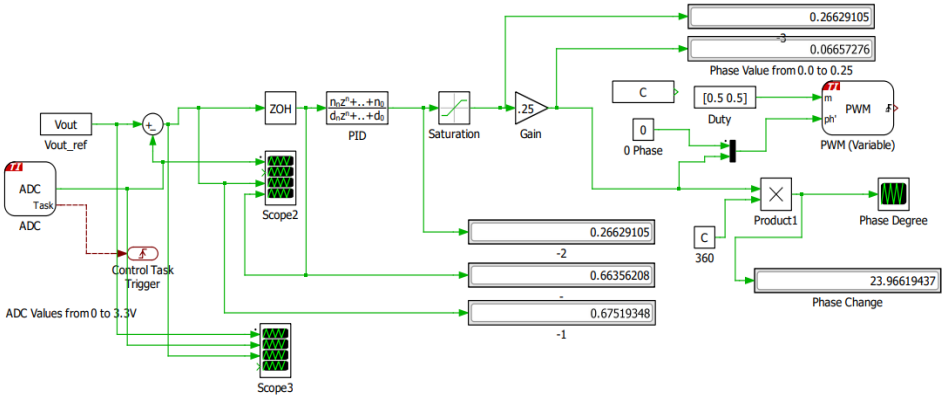


Figure 5.7 Third page of simulation (simulation of control design)

PLCES Simulation software [20] Provides PLECS Coder for Texas Instruments (TI) C2000 microcontrollers (MCUs) and the TI C2000 Target Support Package. The Pulse-width modulator (PWM) peripheral is configured inside the PWM block, where users can provide duty

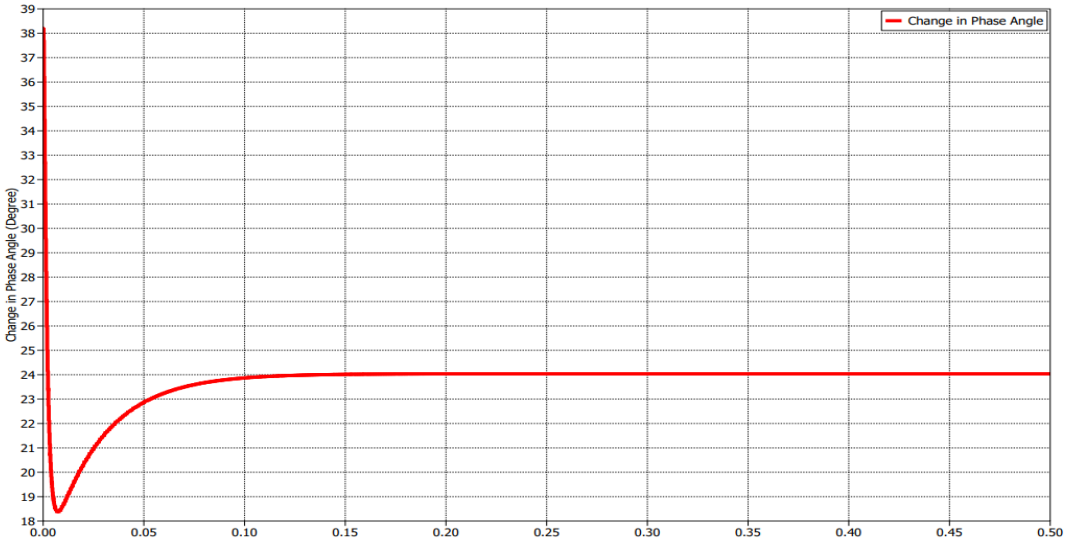


Figure 5.8 Simulation result 4 (changing phase angle)

cycle, carrier type, carrier frequency, and Blanking time (dead). When a program runs, the PWM signals are generated with a complementary PWM pair, i.e., ePWMxA and ePWMxB; this PWM Block also configures the PWM output pins of the MCU. Similarly, PLCES coders also have ADC Block and DAC Block, which are used to design feedback controllers. Using these blocks, a simulation of the control design is done, as shown in Figure 5.7. The control design in the simulation senses the output voltage and generates an error signal using a reference signal, and then the PID controller is applied to it. The PID controller is used to control the phase shift of PWM signals of the secondary side with reference to the primary side's PWM signals.

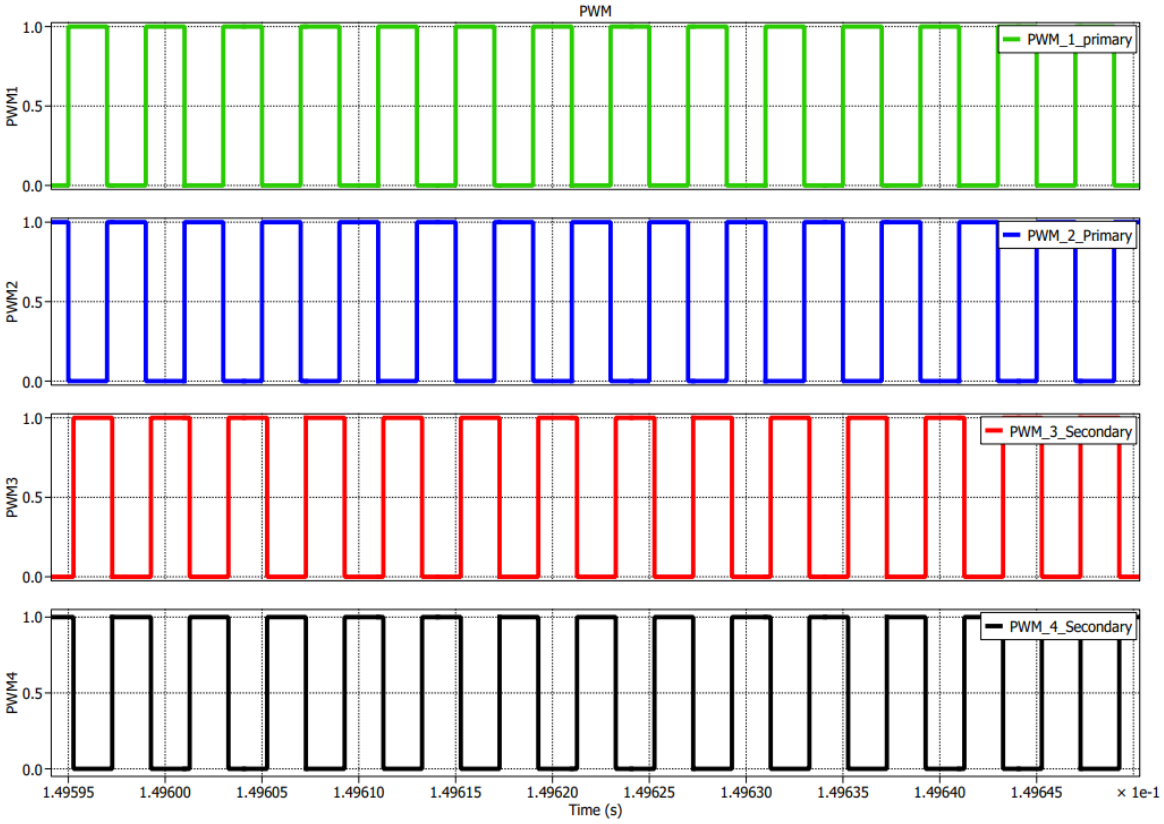


Figure 5.9 Simulation result 5 (PWM signals for Primary and Secondary side Switches)

Figure 5.9 shows generated PWM1 and PWM2, and their complementary signals are applied to primary side switches. Similarly, PWM3 and PWM4 and their complementary signals are applied to secondary side switches; note that the Phase of PWM3 and PWM4 is shifted with respect to PWM1 and PWM2. Figure 5.10 also shows the phase shirt in secondary PWMs compared to primary PWMs signals**.**

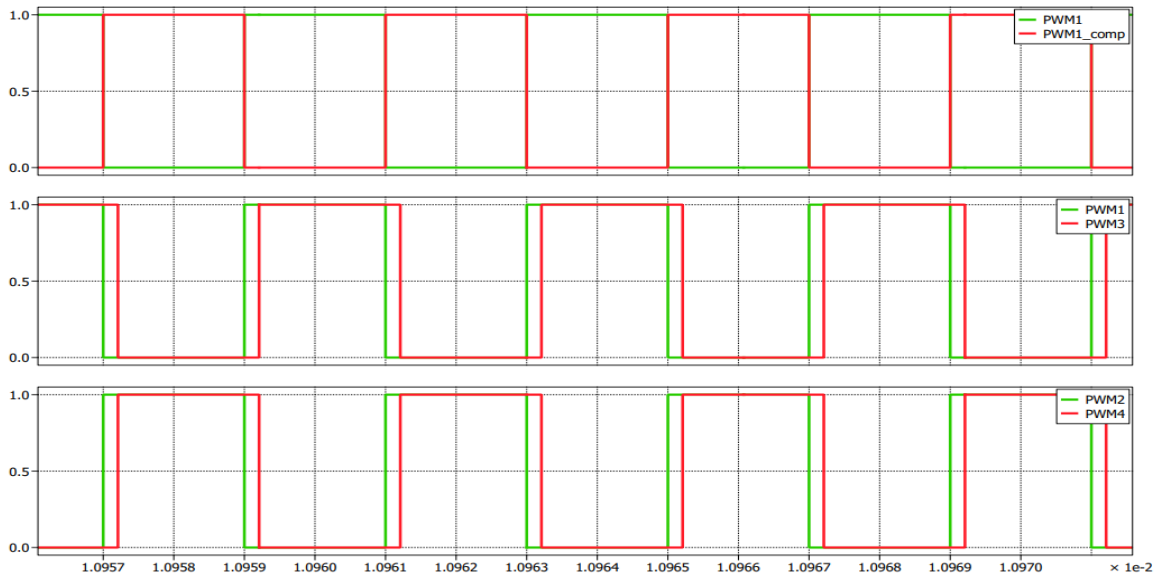


FIGURE 5.10 Simulation result 6 (Phase Shift of PWM signals)

Thermal management is crucial in power electronics systems to analyze the performance parameters of power module packaging, which is crucial for high-density power electronics systems [21]. PLECS allows the simulation of heat sink design, and on the other hand, it also enables the finding of switching and conduction losses and junction temperature of the device. To calculate the switching losses, PLECS uses a 3D look-up table from the thermal library, records operating conditions, and compares it with the loop-up table. Figure 5.11 shows the thermal library of the GaN system (GS66516).

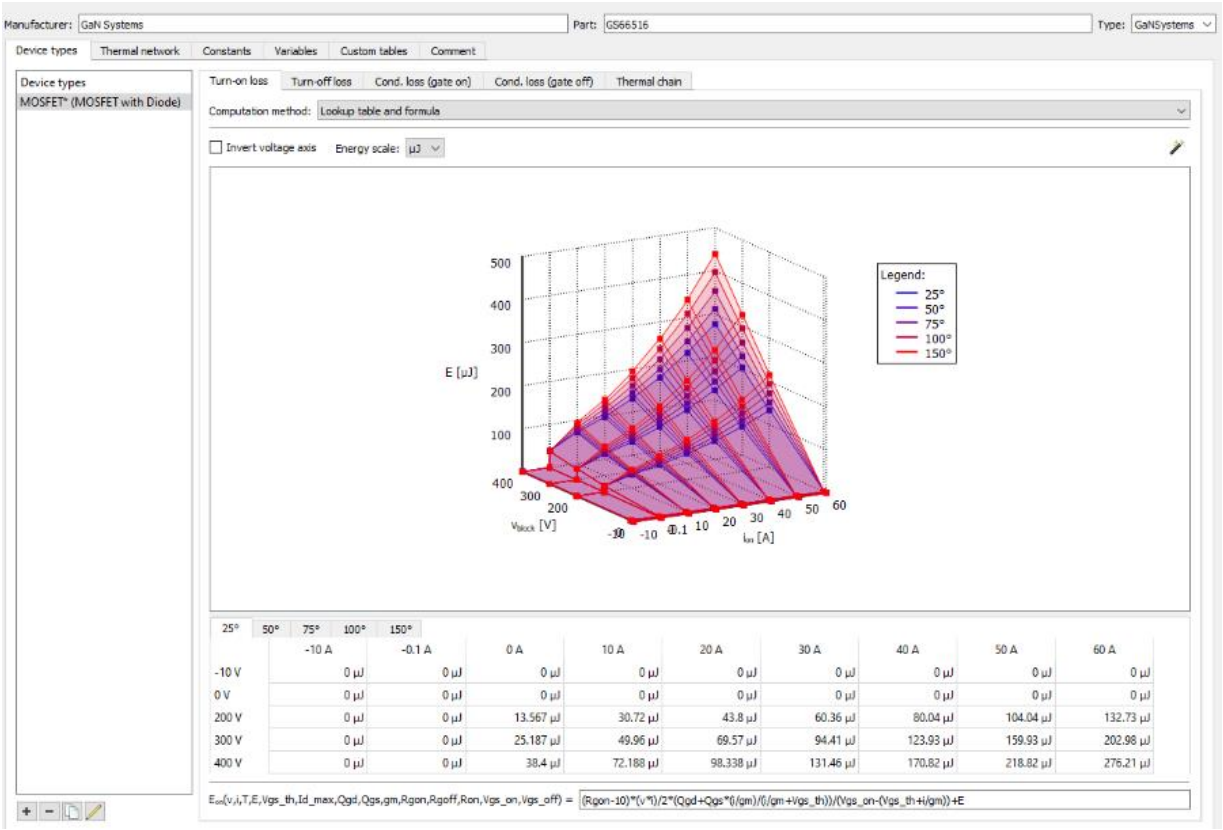


Figure 5.11 3D look-up table from the thermal library.

The thermal library also allows the simulation of a heat sink, where thermal structural modeling can be done by adding details such as ambient temperature, thermal conductivity of the material, thermal resistance, and capacitances. Figure 5.12 shows the heat sink depicted.

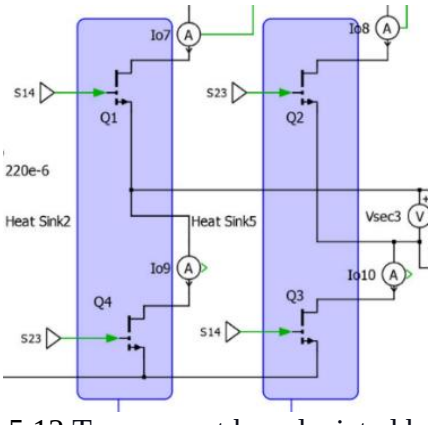


Figure 5.12 Transparent box depicted heat sink.

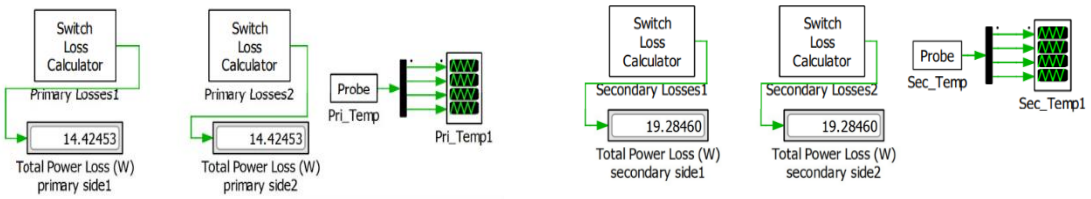


Figure 5.13 Power losses in primary side and secondary side switches.

Figure 5.13 shows the proposed converter's total power losses: 28.84906 watts on the primary side and 38.5692 watts on the secondary side. Figures 5.14 and 5.15 show the junction temperature in the primary and secondary devices when the output power is 5129 watts.

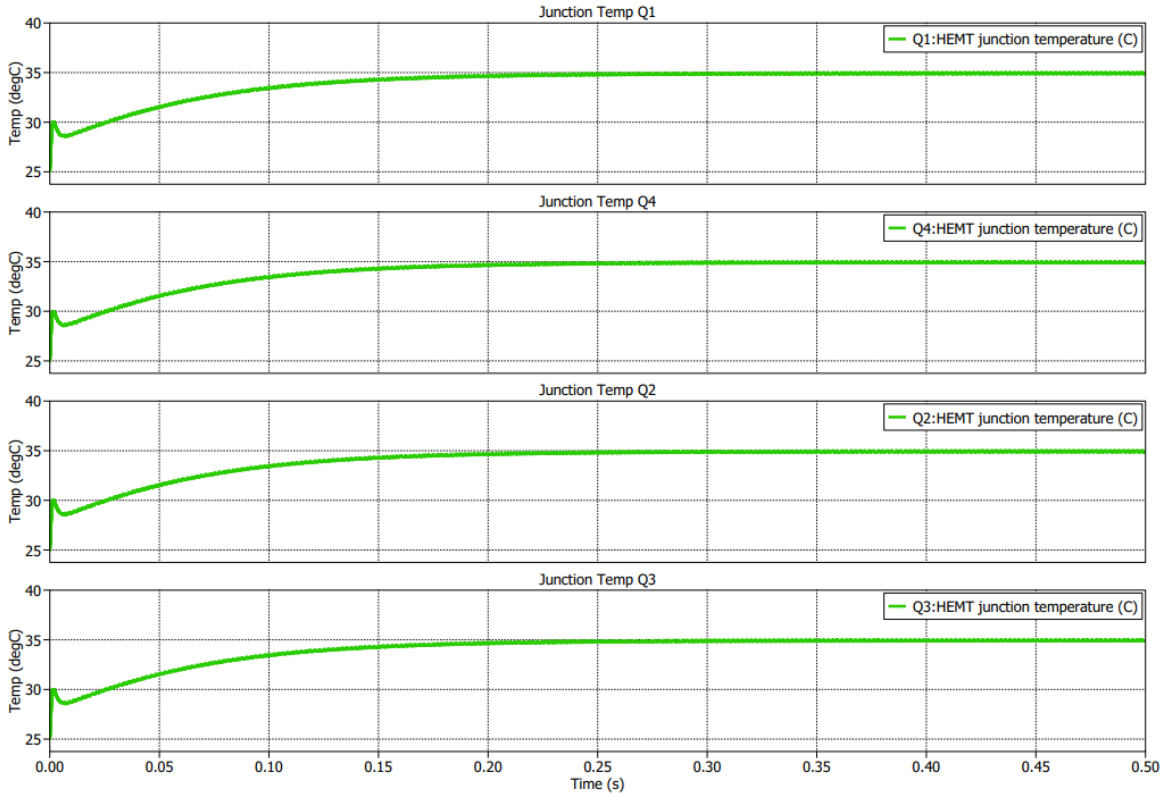


Figure 5.14 (Simulation result 7) Junction temperature of primary side GaN devices.

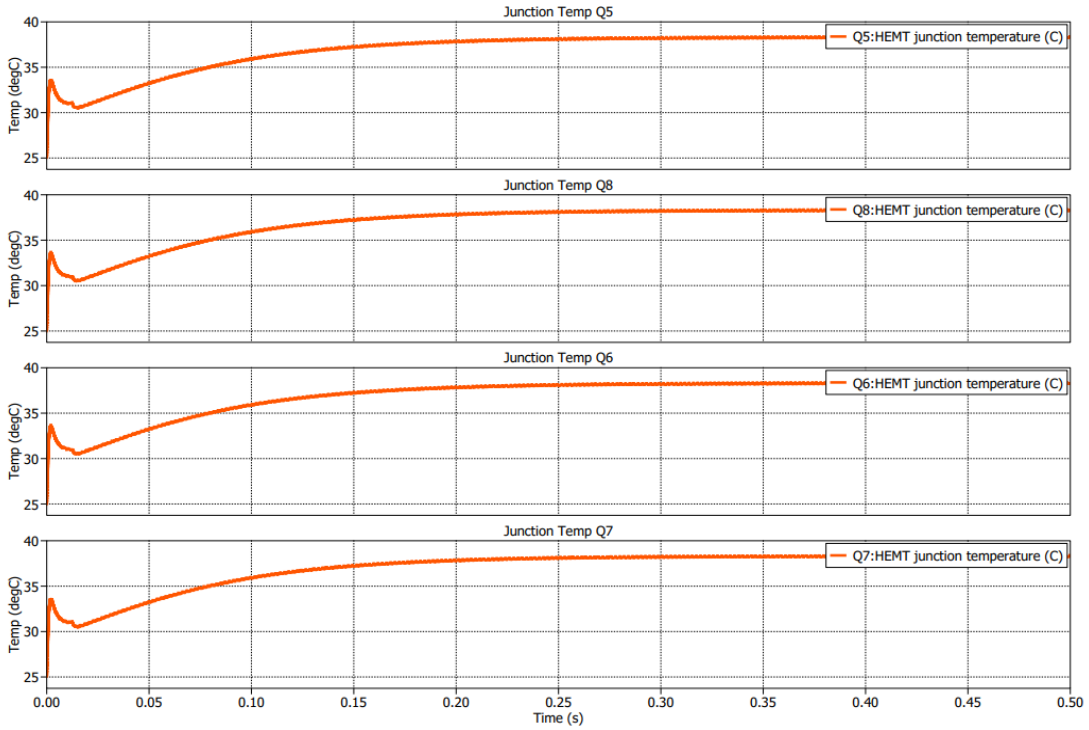


Figure 5.15 (Simulation result 8) Junction temperature of secondary side GaN devices.

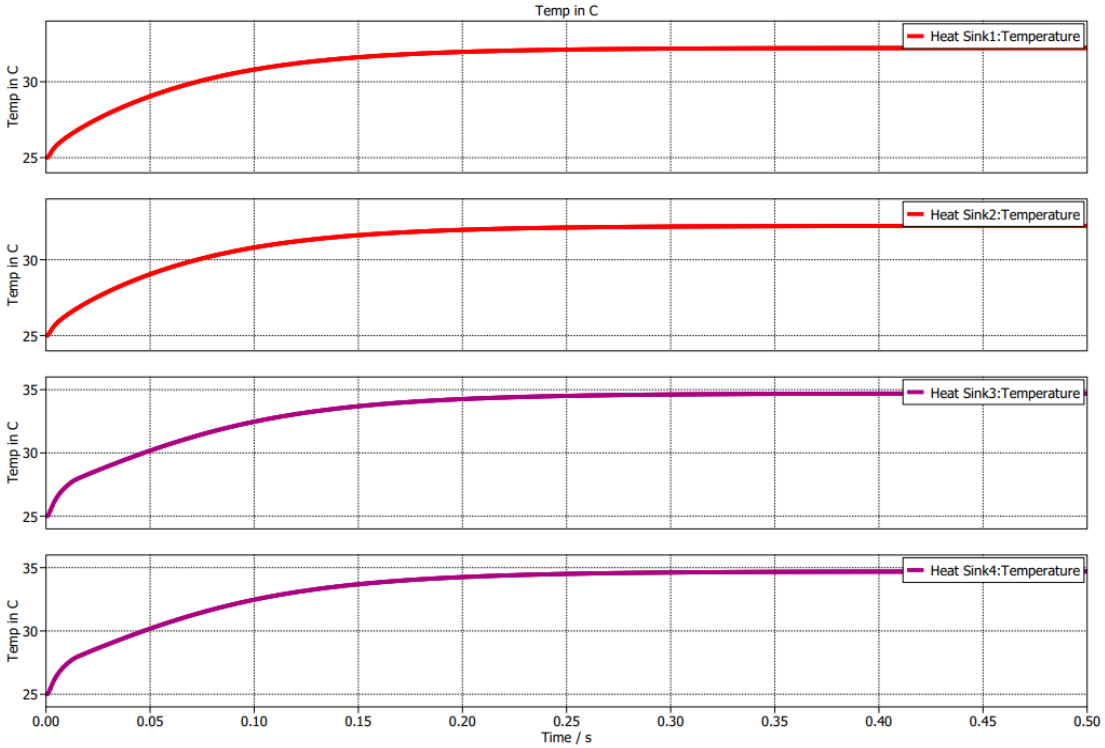


Figure 5.16 (Simulation result 9) Temperature of heat sinks while operating.

5.3 Feedback Controller Design

The power flow of a dual active bridge depends on the phase change; therefore, to control power, a single-phase shift modulation technique is most common. There are a variety of control schemes to control dual active bridges, such as single-phase shift, dual-phase shift modulation, triple-phase shift modulation, and hybrid-phase shift modulation [22] . This variety of methods offers many benefits, but their controller design and implementation are much more complex; therefore, single-phase shift modulation is very simple to implement for controlling this converter [23]. The output voltage of the dual active bridge used for EV battery charging should be controlled to maintain uninterrupted power flow in a direction. On the other hand, the battery of an EV also works as a source for a vehicle to grid power flow (in the reverse direction). Hence, the output voltage should be regulated to prevent undesirable power flow in the opposite direction, as a converter is designed to work in a bidirectional power flow. Therefore, it is crucial to monitor and regulate input/output voltage and current using a PI controller to control the phase shift modulation techniques to control power flow. The feedback control loop (PI or PID control) of a power converter can be understood by following Figure 5.17, where G(s) is the plant or converter, C(s) is the controller, Vref is the set point of a reference signal (which 250 V in this converter design), and Vout is measured output voltage which fed back to the input. Compared with a reference voltage, the difference between reference and output is known as error signals. The controller uses this error signal as input, tries to control the plant, and finally generates output voltage. It eliminates the error, effectively realizing zero steady-state error. Since a dual active bridge is considered a first-order system [24], the PI controller is sufficient to implement to achieve almost zero steady error in the design. The transfer function of the plant can be written in the s domain using the Laplace transform [24] as in equation (5.4), where K is the gain, T is the time constant, and the transfer

function of the PI controller is shown in equation (5.5) where Kp is the proportional gain. Ki is the integral gain.

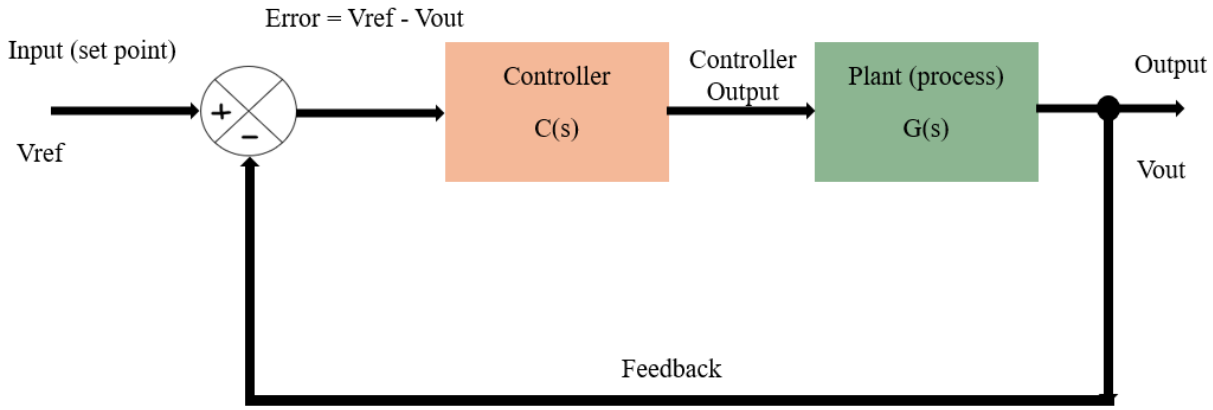


Figure 5.17. Closed loop feedback controller

$$G(s) = \frac{K}{sT+1} \tag{5.4}$$

$$C(s) = K_p + \frac{K_i}{s} \tag{5.5}$$

The final input and output characteristics can be written using the above transfer function.

$$H(s) = C(s)G(s) = (\frac{K}{sT+1})(\ K_p + \frac{K_i}{s}\ ) \tag{5.6}$$

Figure 5.18 shows the PI controller's response when the load changes from 50% to 100%. The PI controller maintains the output voltage in the PLCES simulation.

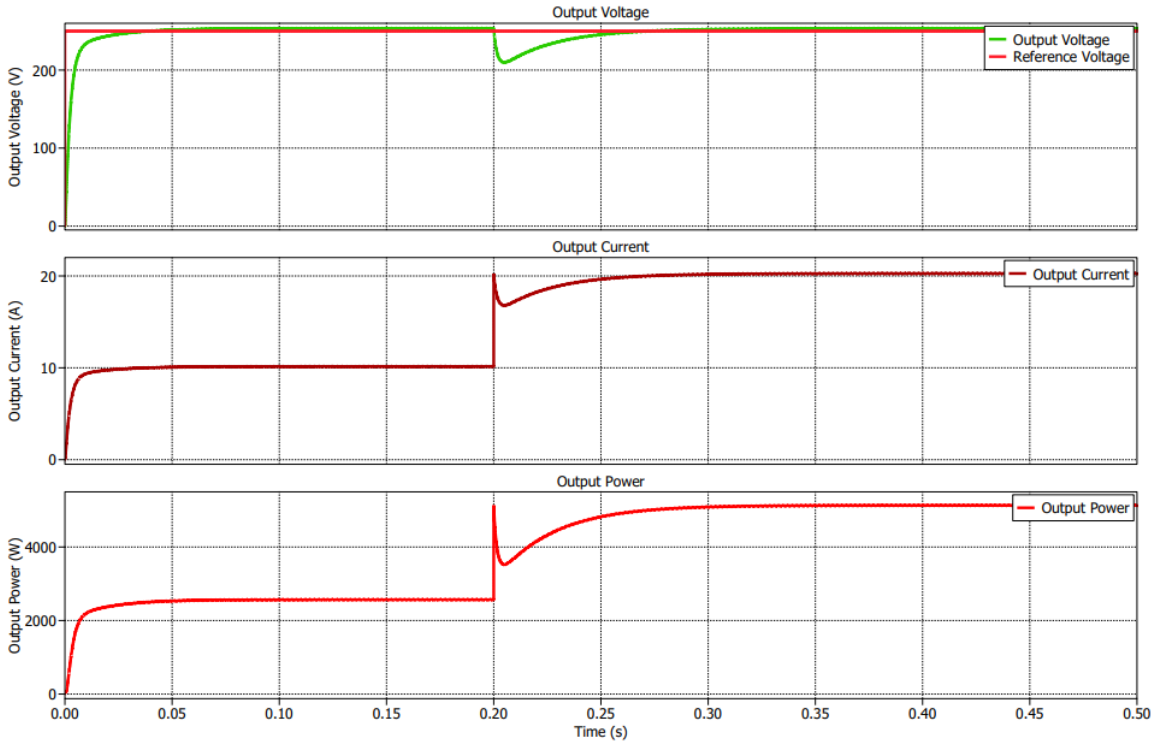


Figure 5.18 (Simulation result 10) Response of PID controller.

5.4 Schematics and PCBs Design for Converter

Designing PCBs for a high-frequency converter involves various challenges, such as Electromagnetic interference (EMI) problems related to mechanical reliability, thermal management, and signal integrity and cross-talk. [17]; therefore, it becomes very important to design PCBs carefully. The traces and routing design need to be so that it minimizes EMI and maintains signal integrity. For example, trace length needs to be as short as possible as longer traces can act the antennas at high frequency and radiate electromagnetic interference. It is essential to design traces wider and use thicker copper as it has lower inductances, which helps reduce power losses. Also, using via array can help distribute current in power planes, increase current carrying capacities, and reduce the risk of overheating.

For high-power circuits, thicker copper traces, typically starting from 2 oz, are crucial to keep lower resistance for lower power losses and better thermal dissipation. This is required because MOSFETs, inductors, and capacitors on power converters need wider geometry traces to conduct high currents without overheating safely. Additionally, thick copper enables shorter and wider traces to reduce the loop area and hence EMI radiation from high-frequency switching; it also maintains the signal integrity by reducing impedance discontinuity at high frequencies. Thicker copper layers also help to counteract the skin effect, where the current flows mainly through the surface of the traces due to resistive losses in high frequencies. Thicker copper layers are also required for better heat dissipation as higher-power and frequency circuits need to dissipate more heat and provide better mechanical integrity to the board.

On the other hand, a power converter also needs high-frequency control and clock signals to control power switches. It requires extra attention while designing the PCB as it is more susceptible to problem-related signal integrity and EMI. [25]. The signal layers ideally need to be routed in the inner layer and sandwiched between ground and power planes. Avoiding vias is useful to reduce impedance changes and discontinuities in the signal path. Using a decoupling capacitor near power pins and components also helps filter out EMI and stabilize noise. The direct route and shortest path with no sharp corners and right-angle bends for clock signals and control signals layer need to be applied. This layer arrangement minimizes electromagnetic interference and provides an optimal low-impedance return path, both crucial for solid signal integrity.

5.4.1 Schematic design converter circuit

The PCB design involves various subcircuits, such as the primary and secondary voltage and

current sensing circuit, the control card circuit, the auxiliary isolated power circuit for the control and sensing circuit, and the primary converter circuit. This section discusses the main converter circuit design. Figure 5.19 shows the Schematic design of the main converter circuit, which consists of various pages and subcircuits referred to as numbers. TI's guide was used as a reference to design this converter [26].

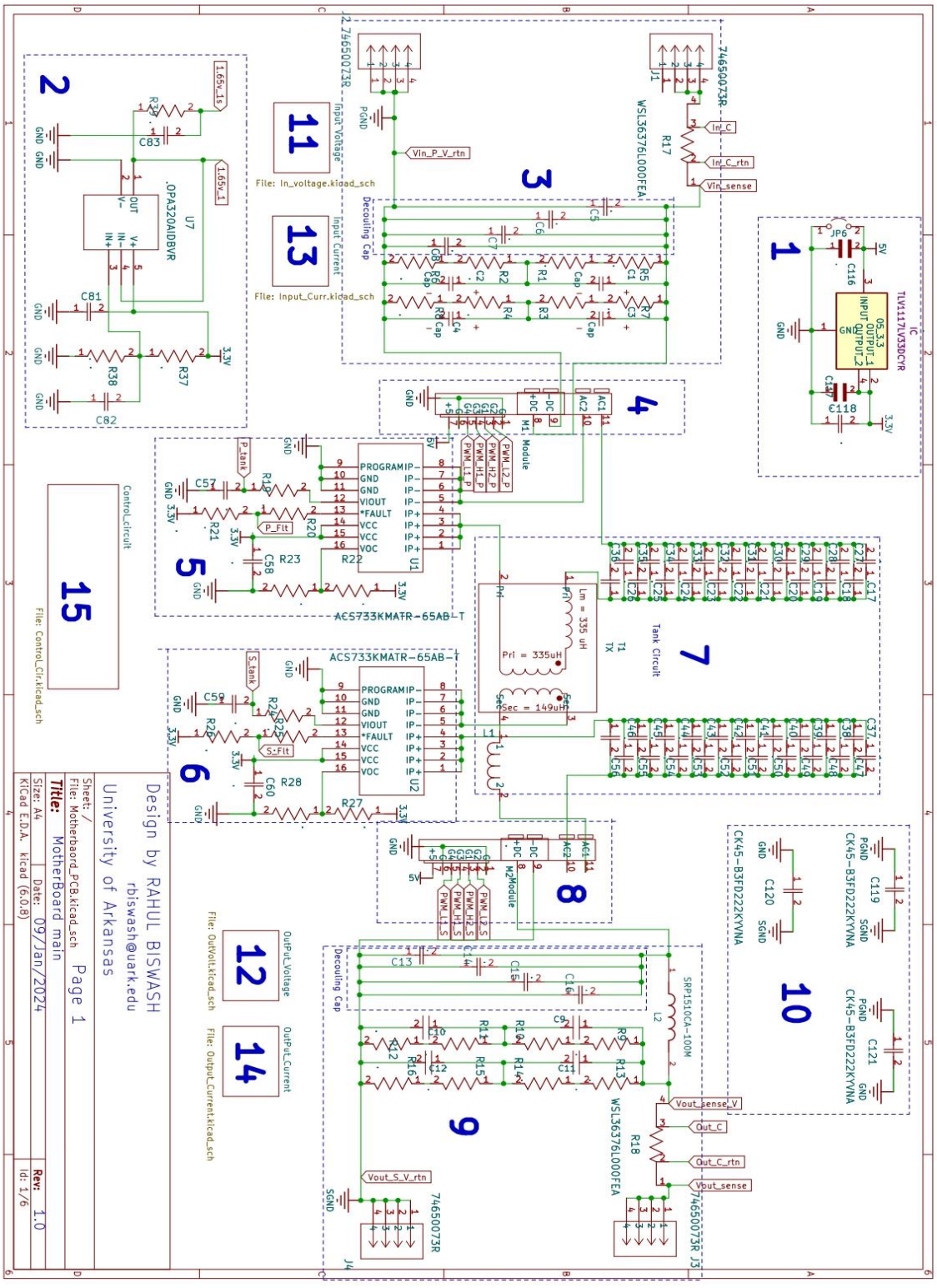


Figure 5.19 Schematic design of the main converter circuit.

(1) The operating voltage for the Control card is 5 V DC, and for the sensor circuit, it is 3.3 V; on the other hand, the reference voltage for the ADC of the control card is 1.65V and 3.3V; therefore, linear voltage regulator IC (TLV1117LV33DCYR) from Taxes Instruments used to convert 5V DC to 3.3V DC.

(2) The TI TMDSCNCD280049C controlCARD's ADC also needs 1.65 V DC. Therefore, to step down, an OpAmp (OPA320AIDBVR) is used. This operational amplifier is optimized for very low noise and wide bandwidth, making it the best choice for ADC design.

(3) The Input DC Link capacitor, combined value 220 uF, is paralleled with a 2 m ohm resistor, which helps reduce input voltage ripple. On the other hand, a 2 m ohm resistor helps reduce the resonant circuit's Q-factor, damping out the capacitor's oscillations. In addition, it has four decoupling ceramic capacitors.

(4) Pad for a primary module, which is further connected to the DC link capacitor (input side), the input of the tank circuit, and the control card's PWM pins.

(5) To sense the primary side tank current ACS733 high isolation, a high-bandwidth Hall-effect-based current sensor detects any fault in the primary side.

(6) To sense the secondary side tank current, an ACS733 high-isolation, high-bandwidth Hall-effect-based current sensor is used, which can also detect any fault on the secondary side.

(7) The tank circuit consists of a high-frequency transformer, capacitor, and series energy inductor.

(8) Pad for a secondary module, which is further connected to the DC link capacitor (output side), the output of the tank circuit, and the control card's PWM pins.

(9) The Output DC Link capacitor, with a combined value of 220 uF, is paralleled with a 2 m ohm resistor, which helps reduce output voltage ripple. On the other hand, a 2 m ohm resistor helps reduce the resonant circuit's Q-factor, damping out the capacitor's oscillations. In addition, it has four decoupling ceramic capacitors.

(10) The high-frequency transformer of a DC-DC converter and PCB always has some parasitic capacitance. This parasite can allow high-frequency noise to circulate between input and output, directly affecting EMI performance and sometimes converter efficiency. This C119, C120, and C121 capacitor provides a low-impedance way to the ground and decouples the input and the outside of the converter. If no such capacitor exists, the high-frequency noise cannot return to the input side and must circulate the converter.

5.4.2 Primary and Secondary Voltage Sensing Circuit Design

To provide feedback to the PID controller and protect it from voltage overshooting, primary and secondary voltages need to be measured; the maximum input voltage it can sense is 800V. In sections (11) and (12) of the schematic design, the input/output voltage circuit was designed, and an IC from the Taxes instrument (AMC1311) was used. AMC1311 consists of an isolation amplifier that separates the input circuit from the output and is highly resistant to magnetic interference;

therefore, this IC can be a good choice for high-frequency converter design. The input circuit of the IC is connected to a resistive divider network, which scales down the Input/Output voltage and feeds to the input of the IC. The output of IC provides differential output, therefore, to an OpAmp TLV9061, which converts it in the range of 0 to 3.3V, and then this voltage is directly fed to the ADC of the control card. Figure 5.20 shows the schematic of the voltage sensor circuit. On the other hand, figure 5.21 shows the DC transfer characteristics of the sensor circuit, which gives an idea of how the output of the sensor circuit changes with high voltage input and output.

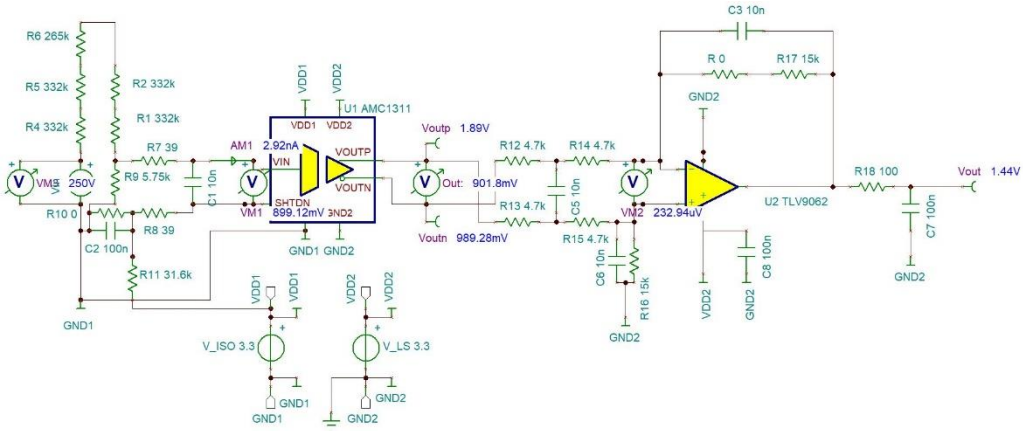


Figure 5.20 Schematic diagram of the primary and secondary voltage sensing circuit.

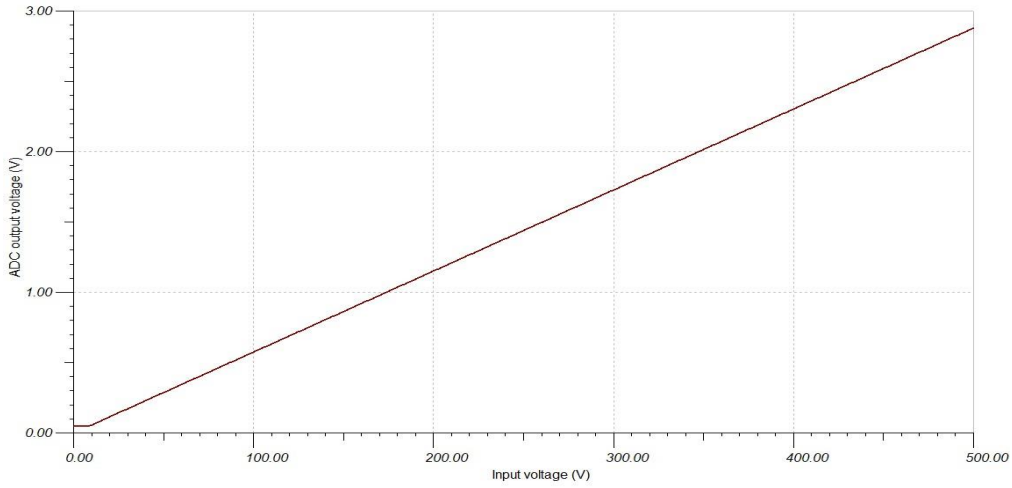


Figure 5.21 DC transfer characteristics of the voltage sensing circuit.

5.5.3 Primary and Secondary Current Sensing Circuit Design.

The input/output current sensing circuit is very important for sensing the overcurrent and providing feedback to the PID controller. In this converter design, a based current sensor is used in section (13) and (14), where very low values 2 m ohm and 1 m ohm, 3 watts shunt resistor connected to the DC terminals and DC voltage across this shunt resistor vary from -50mV to +50mV as input current varies and that this voltage feed to IC AMC3302 then it scaled by a gain factor 41 to produce 2.05V The AMC3302 IC a precise and consist isolated amplifier optimized for shunt based current measurement, further this output voltage scaled and level shift by the OpAmp in the range of 0 -3.3 V for ADC.

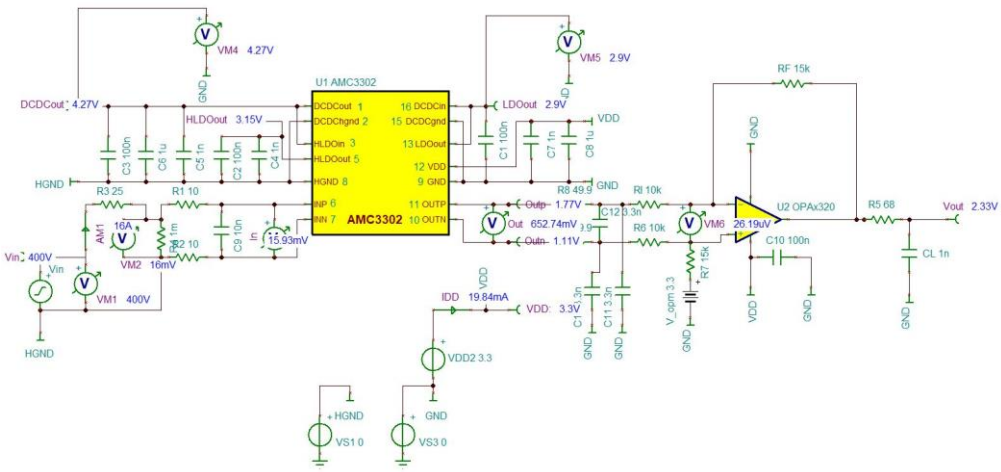


Figure 5.22 Schematic diagram of the primary and secondary current sensing circuit

Figure 5.22 shows the primary and secondary current sensing circuit. The only difference between the primary and secondary sensors is that the shut resistor for the primary side uses 2 ohm, and for the secondary side, it is 1 ohm. On the other hand, Figures 5.23 and 15.24 show the DC transfer characteristics of the current sensing circuit where the sensor's output voltage varies with

voltage changes across the shunt resistor when the current changes in the input and output side of the converter.

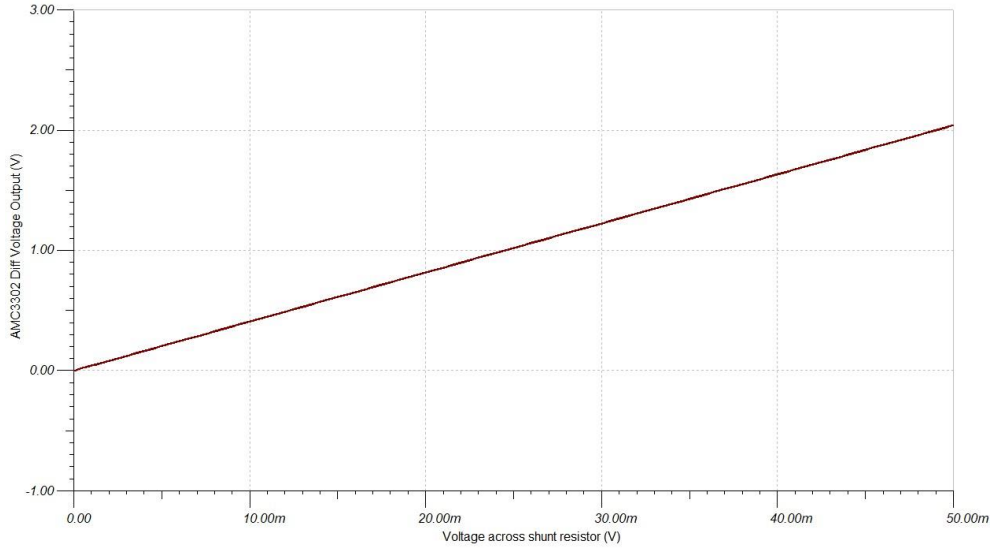


Figure 5.23 DC transfer characteristics of current sensing IC AMC3302

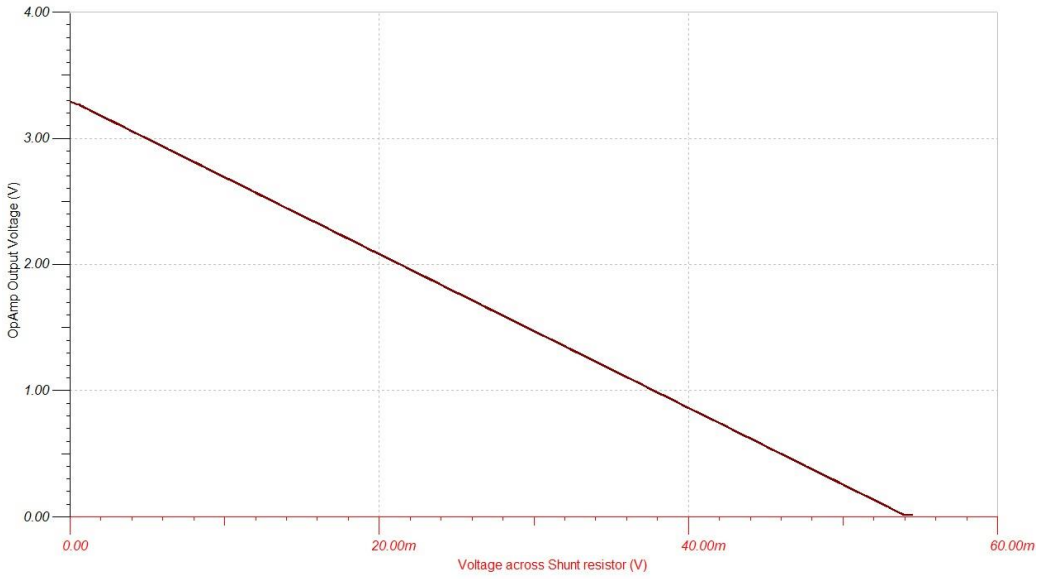


Figure 5.24 DC transfer characteristics of current sensing circuit with OpAmp.

5.5.4 Auxiliary isolated power circuit design for the sensing circuit

For safety reasons, an auxiliary isolated power circuit was designed for the sensing circuit. All operational amplifiers and ICs used operate at 3.3V, and the control card operates at 5 V; therefore, two Isolated DC-DC Converter Modules, one output 3.3V, 303mA, and Inputs 4.5V—5.5V, were used to design this circuit. Figure 5.25 shows the schematic for the Auxiliary isolated power circuit.

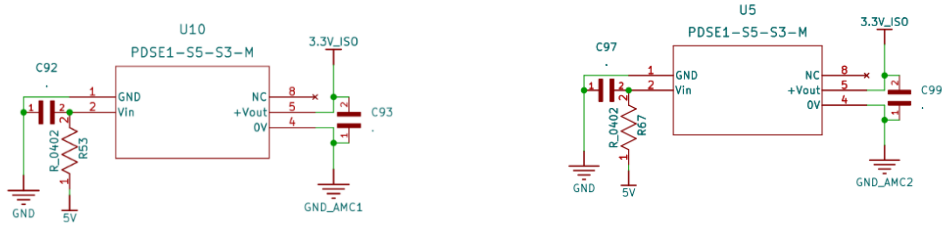


Figure 5.25 Schematic diagram of auxiliary isolated power circuit design for the sensing circuit.

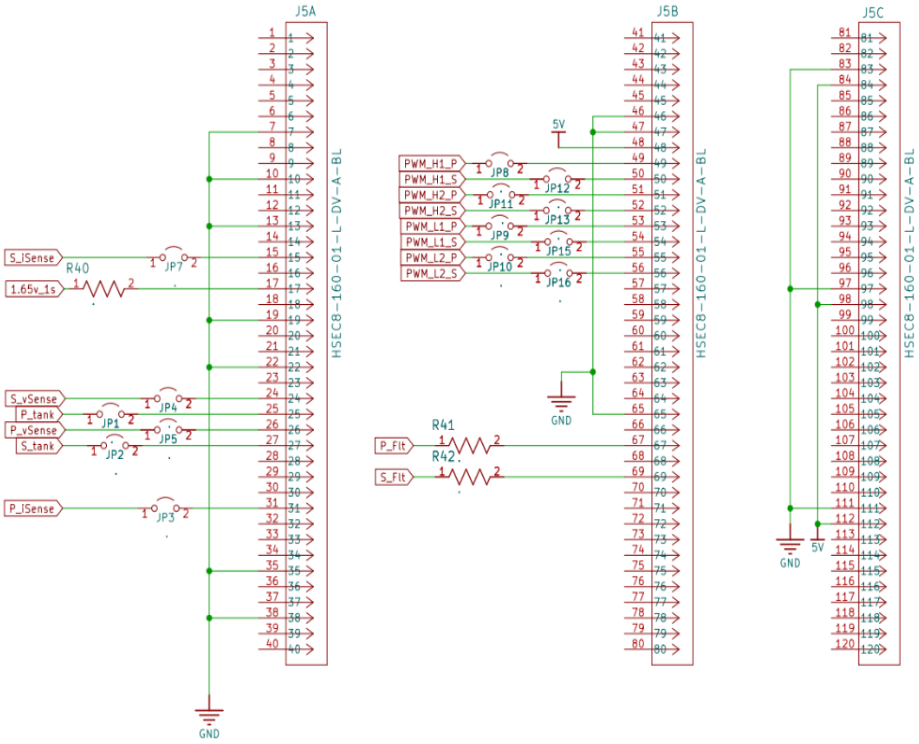


Figure 5.26 Schematic diagram control card connector.

Figure 5.26 shows the schematic diagram of the control card connector, which provides the

connection interface for all eight PWM pins from the Power Module connected to the control card's ePWM pins and connections for the control card's ADCs. It is referred to as number (15) in the main schematic drawing shown in the above figure.

After a schematic drawing of all sections with libraries of components, the PCB was designed as per the details mentioned previously for high-frequency design. The PCB is a six-layer board. All power traces are wide and have an array of vias for current distribution, and the high-frequency PWM signals are sandwiched between 5 V and a ground plan, which provides good noise immunity to them. Figure 5.27 shows the top layer (Red color) and bottom layer (Blue color) of the PCB design.

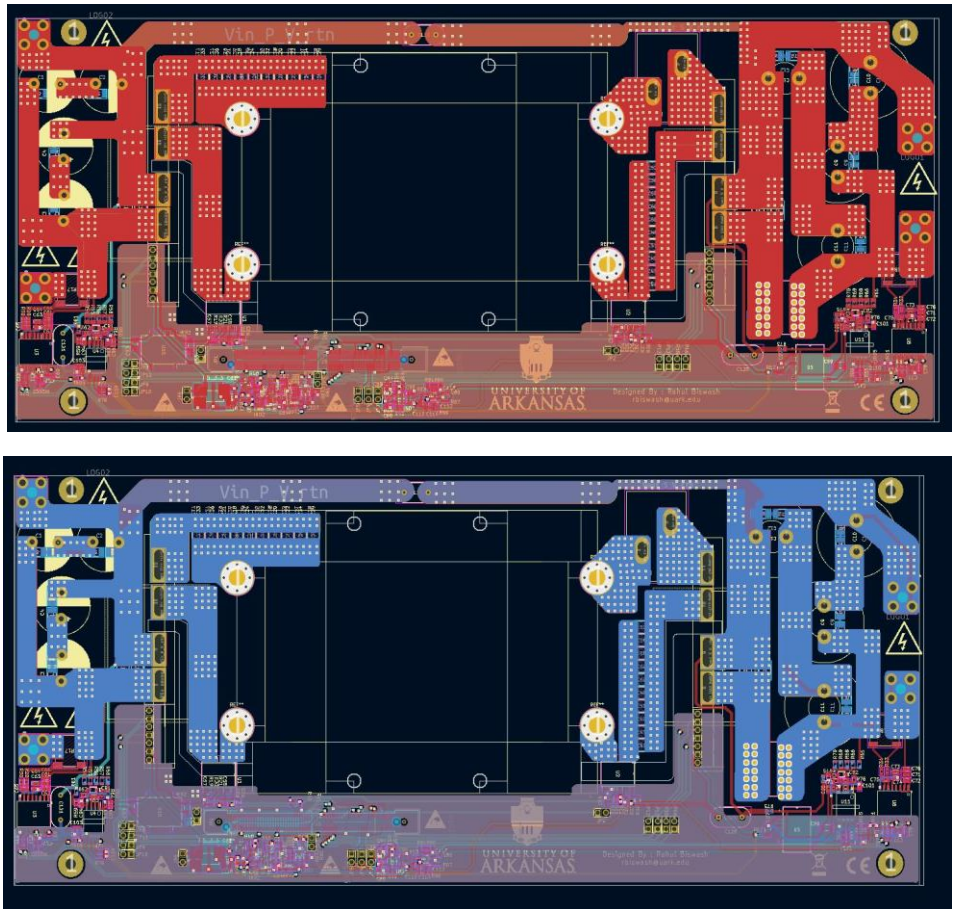


Figure 5.27 PCB design of the main board.

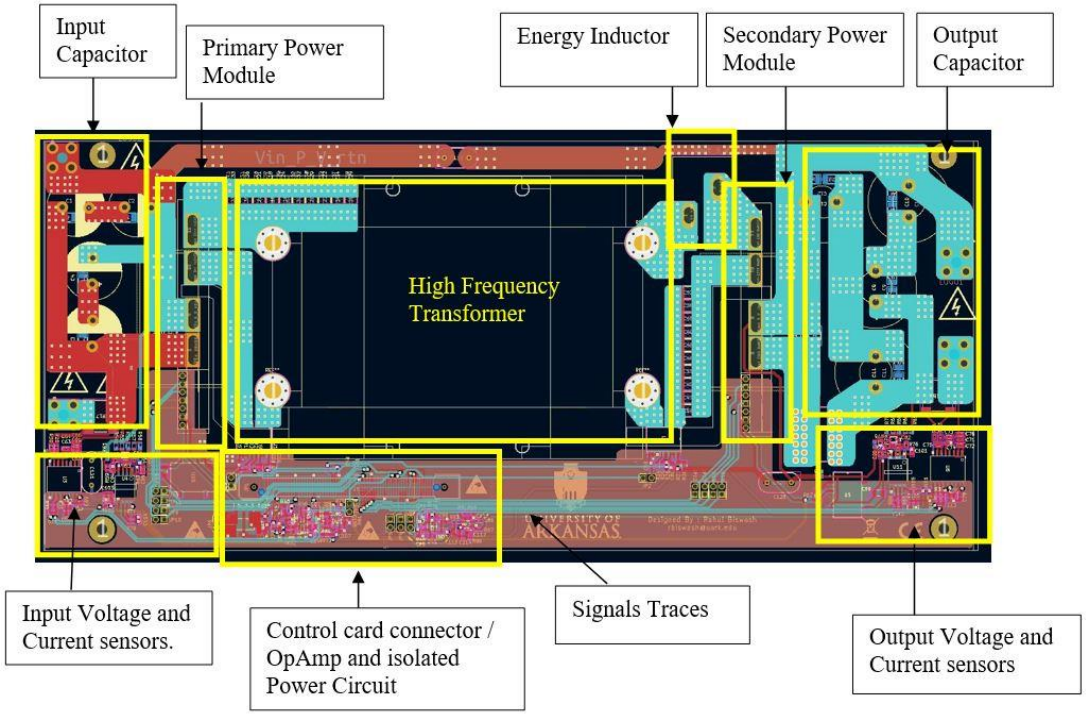


Figure 5.28 Signal layer of PCB design of the main board.

Figure 5.28 shows layer 2 (signal layer) and indicates all sections of the PCB design. On the other hand, Figure 5.29 shows a zoomed picture of the input current and voltage sensor circuit in the PCB design. Similarly, Figure 5.30 shows a zoomed image of the output voltage and current sensor circuit. Figure 5.31 shows the PCB of the control card connector and all the OpAmp circuits of the voltage and current sensors.

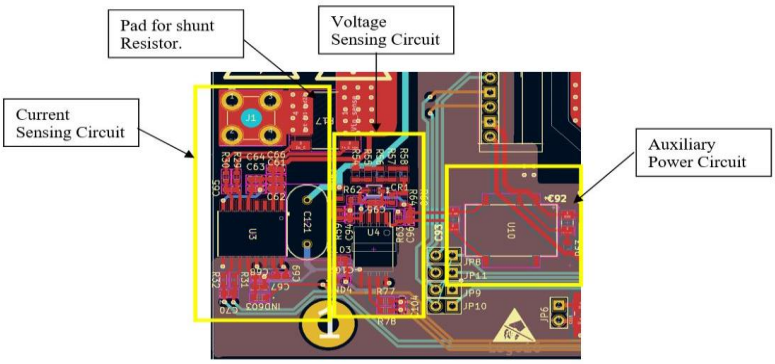


Figure 5.29 PCB design of input current and voltage sensor circuit.

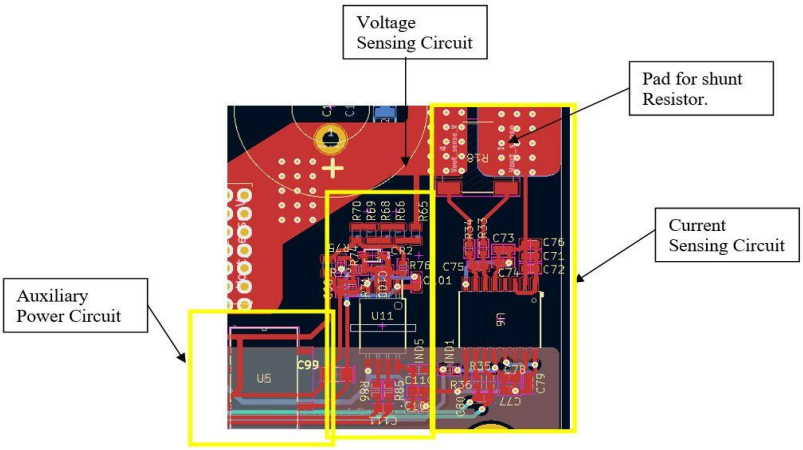


Figure 5.30 PCB design of output current and voltage sensor circuit.

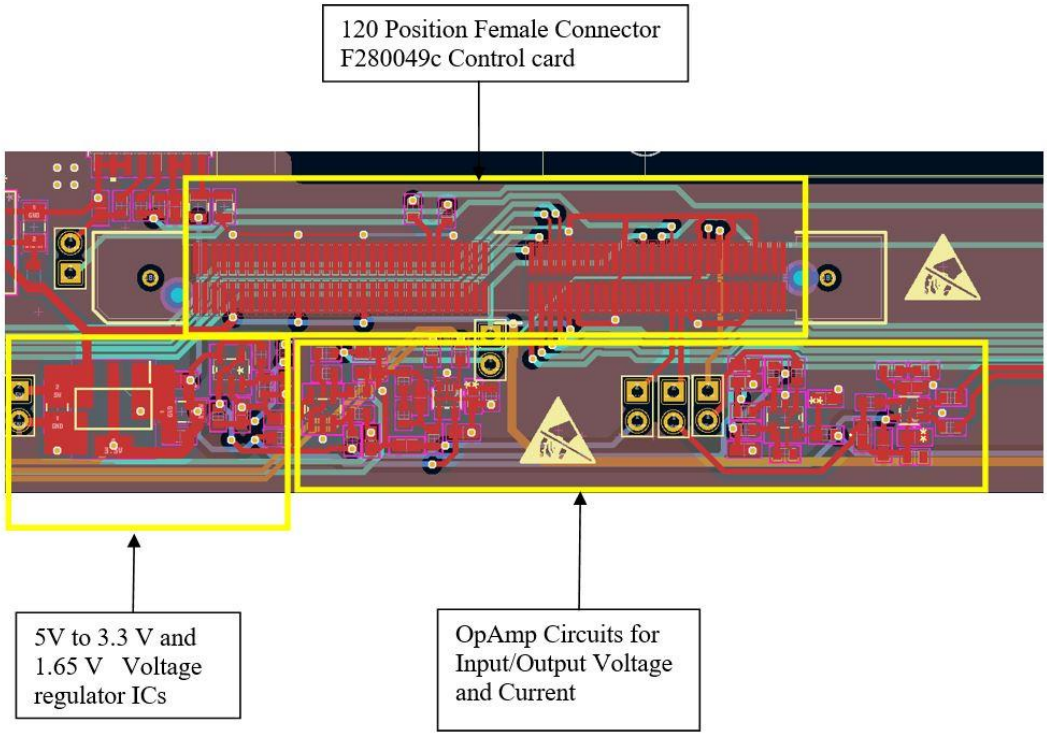


Figure 5.31 PCB design of control card connector and OpAmp circuit.

Figures 5.32 and 5.33 show the 3D CAD file of the PCB design for the converter's top and Bottom sides.

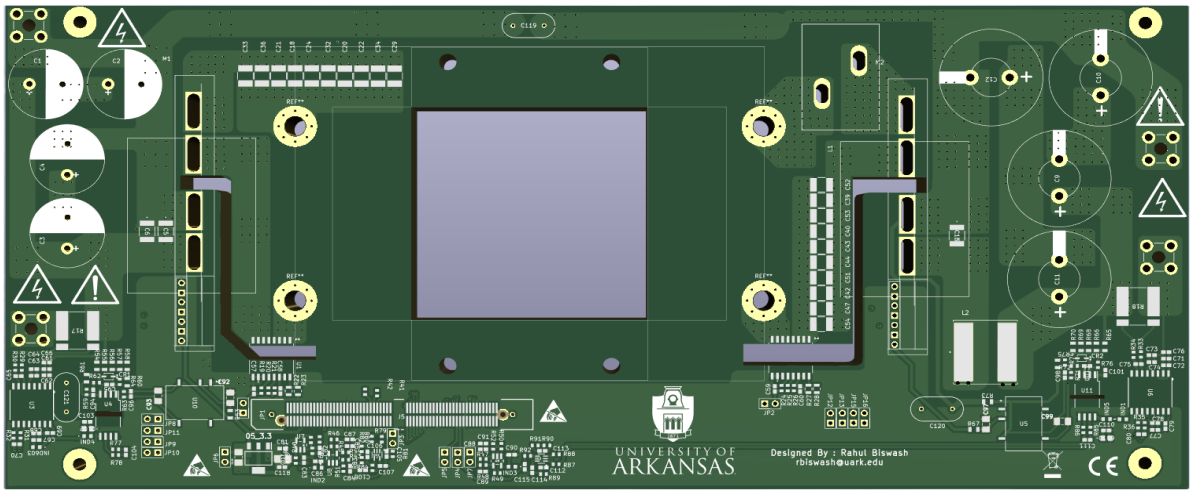


Figure 5.32. 3D CAD file of PCB design (Top Side)

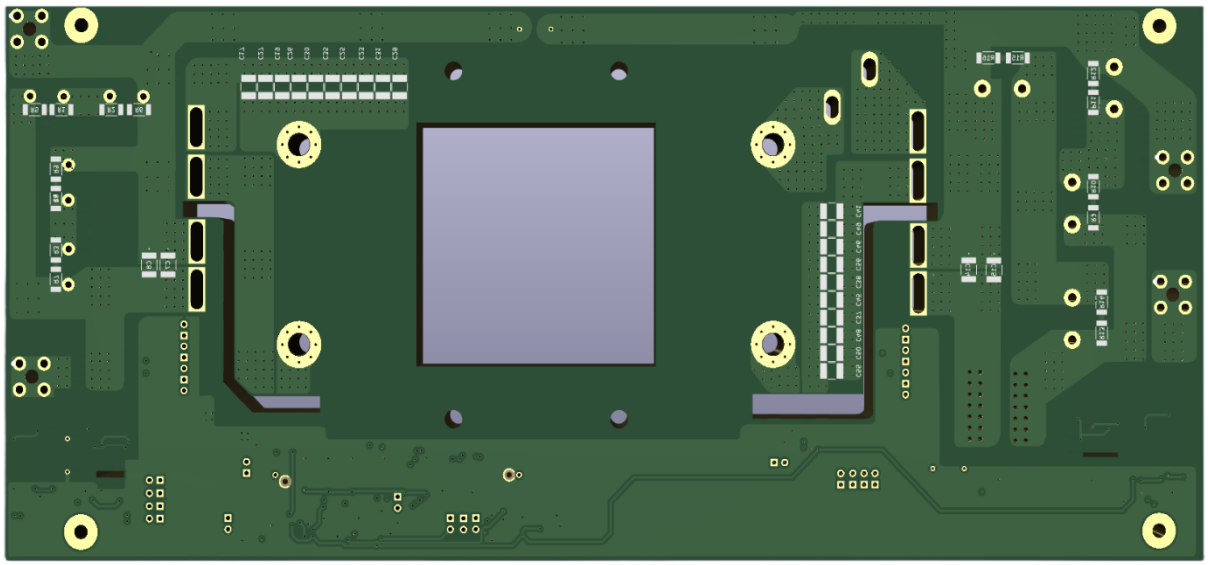


Figure 5.33. 3D CAD file of PCB design (Bottom-Side)

5.6 Implementation of digital control using TI F280049C Control Card

The implementation of digital control involves generating PWM signals from the ePWM peripheral, measuring ADC signals, and controlling Phase shift with a PI Controller based on ADC signals using TI C2000 DSP F280049C control card; before implementing coding, it is essential to know the pin configuration control card and its functionalities. To properly function the system, calibration needs to be done with the components mounted on the PCB. Sometimes, troubleshooting becomes very challenging when coding and calibration are not adequately aligned with the design.

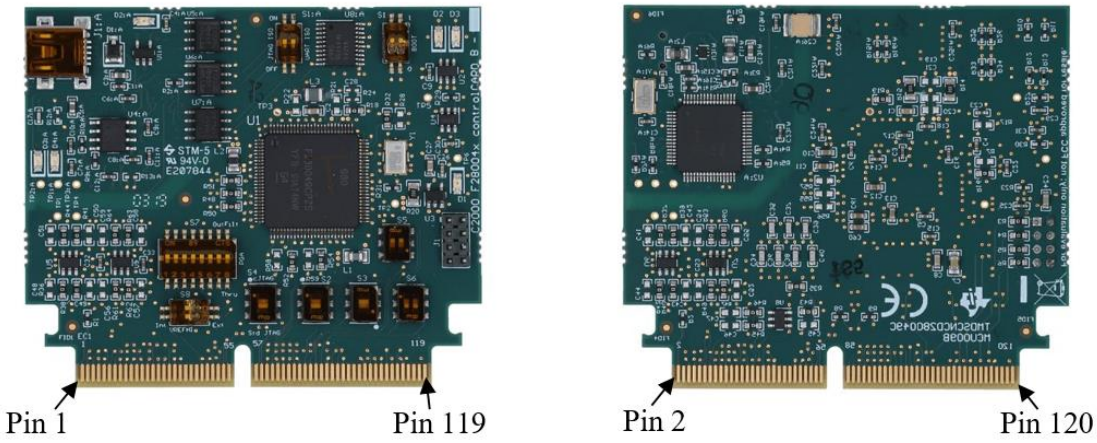


Figure 5.34 TI C2000 DSP F280049C control card

For Developing and testing high-performance, high-frequency power converters, the F280049 controlCARD control systems are a good choice, as shown in Figure 5.34, because the F28004x family microcontroller has advanced processing, control, and safety features. The controlCARD exposes these advanced microcontroller features through the 120-pin HSEC8 edge connector. This HSEC8 interface helps achieve fast prototyping and evaluation of the F28004x device for high-frequency power converter design. The many features of this board are mentioned in the referred datasheet. [27] .

Figure 5.35 GPIO pins of TI C2000 DSP F280049C control **[28]**

Pin Name	Pin Number	Description	GPIO	ADC
A0 (P_vSense)	9	Primary Voltage Sense	-	C0 (26)
A1 (S_vSense)	11	Secondary Voltage Sense	-	B4 (24)
A2 (S_iSense)	15	Secondary Current Sense	-	B6 (15)
A3	17	1.65 V Reference	-	-
A5 (P_iSense)	23	Primary Current Sense	-	C5 (31)
A6 (P_tank)	25	Primary Tank Sensor	-	-
A9 (S_tank)	27	Secondary Tank Sensor	-	-
PWM-1A	49	Primary Leg-1 High Side	GPIO-00	-
PWM-1B	51	Primary Leg-1 Low Side	GPIO-01	-
PWM-2A	53	Primary Leg-2 High Side	GPIO-02	-
PWM-2B	55	Primary Leg-2 Low Side	GPIO-03	-
PWM-3A	50	Secondary Leg-1 High Side	GPIO-04	-
PWM-3B	52	Secondary Leg-1 Low Side	GPIO-05	-
PWM-4A	54	Secondary Leg-2 High Side	GPIO-06	-
PWM-4B	56	Secondary Leg-2 Low Side	GPIO-07	-

Table 5.2 shows the PIN of the GPIO and ADC with a description.

Figure 5.35 shows the GPIO pins of TI C2000 DSP F280049C, and Table 5.2 shows the pins with descriptions used for programming and writing code. TI's IDE code composer studio is used for C2000 DSP programming.

Generally, PWM signals are generated by comparing a carrier signal with a reference signal, as shown in Figure 5.36. In MCUs, there are no analog signals; therefore, it uses up-down count mode as carrier signals. It starts counting from zero and increments until the TBPRD (time-based period) reaches and then decreases to zero, as shown in Figure 5.37 [29] .

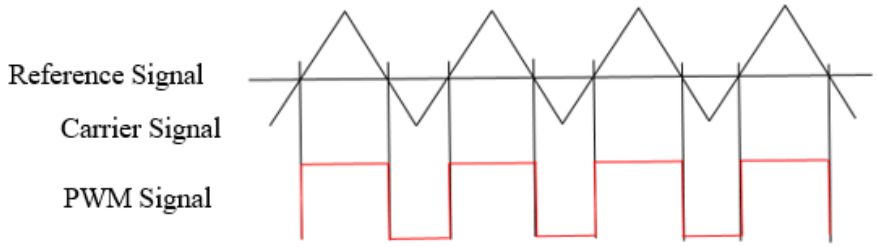


Figure 5.36 PWM waveform using reference and carrier signals.

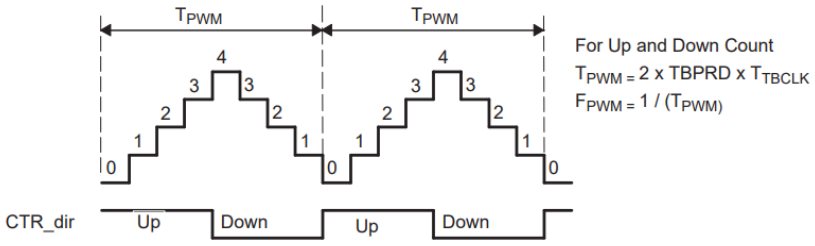


Figure 5.37 Up-down count mode as carrier in DSP

This TBPRD is used to determine the frequency of PWM signals in DSP programming. Equation (5.7) is used to determine its value. For example, the clock frequency for the F280049C board is 100Mhz, so to generate 250Khz, the TBPRD needs to be 200.

$$F_{PWM} = \frac{1}{T_{PWM}} = \frac{1}{2 \cdot TBPRD \cdot T_{TBCLK}} = \frac{F_{CLK}}{2 \cdot TBPRD} = \frac{100}{2 \cdot (200)} \text{MHz} = 250\text{kHz} \quad (5.7)$$

The PID controller mentioned above cannot be directly implemented as it is in the control card; it needs to be converted to discrete-time representation from its continuous time representation to implement using C programming; the equation (5.8) represents the PID controller in the s domain.

$$PID(s) = K_p + \frac{K_i}{s} + K_d s \quad (5.8)$$

Z transform of the above equation with sampling time Ts represents its discrete domain; the sampling time needs discretization as the intervals at which the system's inputs and outputs are measured and updated. On the other hand, N is the filter coefficient used to improve the performance of the derivative term.

$$PID(z) = K_p + \frac{K_i T_s z}{z-1} + \frac{K_d N(z-1)}{(1+NT_s)z-1} \quad (5.9)$$

The equation (5.9) is described in z transform and discrete format, but to implement it in DSP programming, it still needs to be rewritten as a differential equation. The standard form of discrete-time PID controller will be.

$$PID(z) = \frac{\Delta(z)}{e(z)} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \quad (5.10)$$

The PID(z) represents the transfer function of the PID controller, where $\Delta(z)$ represents the Laplace transform f the derivative of the control signal, and $e(z)$ represents the Laplace transform of the error signal. On the other hand, a_0 a_1 a_2 b_0 b_1 and b_2 are the coefficients.

The partial fraction decomposition and inverse z transform of equation (5.10) can be written and expressed as $\Delta(k)$ in terms of $e(k)$ Which is a discrete-time sequence that can easily be implemented in coding.

$$\frac{\Delta(z)}{e(z)} = \frac{A}{a_0} + \frac{B}{a_1} + \frac{C}{a_2} \quad (5.11)$$

Equation (5.11) is expressed in the sum of partial fractions of equation (5.10) and multiplied on both sides with $e(z)$, Which gives equation (5.12)

$$\Delta(z) = \frac{Ae(z)}{a_0} + \frac{Be(z)}{a_1} + \frac{Ce(z)}{a_2} \tag{5.12}$$

To find a discrete time sequence, the inverse z transform applied to equation (5.12) can simplified more in the form of equation (5.14)

$$\Delta[k] = \frac{Ae[k]}{a_0} + \frac{Be[k-1]}{a_1} + \frac{Ce[k-2]}{a_2} \tag{5.13}$$

$$\Delta[k] = \frac{-a_1}{a_0}\Delta[k-1] - \frac{a_2}{a_0}\Delta[k-2] + \frac{b_0}{a_0}e[k] + \frac{b_1}{a_0}e[k-1] + \frac{b_2}{a_0}e[k-2] \tag{5.14}$$

Further, the value of coefficients can be found as follows.

$$a_0 = (1 + NT_s) \tag{5.15}$$

$$a_1 = -(2 + NT_s) \tag{5.16}$$

$$a_2 = 1 \tag{5.17}$$

$$b_0 = K_p(1 + NT_s) + K_iT_s(1 + NT_s) + K_DN \tag{5.18}$$

$$b_1 = -\left(K_p(2 + NT_s) + K_iT_s + 2K_dN\right) \tag{5.19}$$

$$b_2 = K_p + K_dN \tag{5.20}$$

Equations (5.15) to (5.20) can be written in C programming and applied to DSP programming. APPENDIX[D] shows the DSP coding.

5.7 Assembly of the converter

The Converter is assembled using various reflow soldering techniques. Initially, the components of the auxiliary power supply, opamp circuit, Control card connector, voltage and current sensor circuit, DC link capacitor, and other passive components are attached to the main board using SAC 305 solder paste. After that, the GaN power modules are soldered together using solder paste on the primary and secondary sides of the Converter. Finally, 5mm nuts and bolts attach the high-frequency transformer to the PCB pad.

Figure 5.38 Designed and Implemented Converter.

CHAPTER 6

EXPERIMENTAL RESULTS

6.1 Test Setup

The experimental test is required to evaluate the performance of the dual active bridge. This will provide insights into overall performance parameters such as losses, efficiency, and thermal data for the converters. Figure 6.1 below illustrates the test setup for high power.

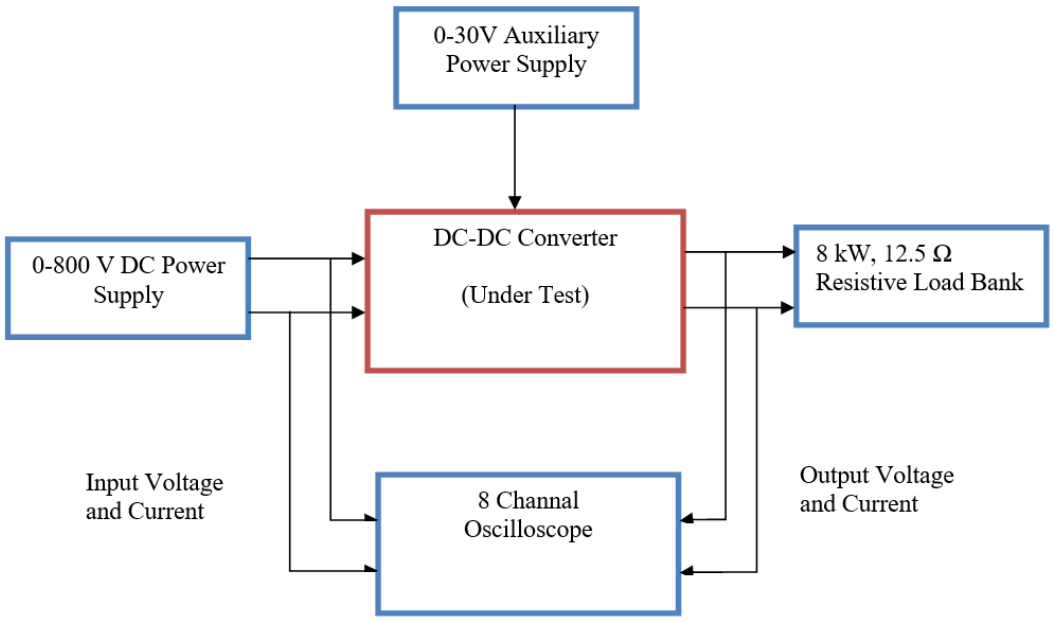


Figure 6.1 Test setup for high power test.

6.2 Low-power test

The tests were conducted in the National Center for Reliable Electric Power Transmission (NCREPT) facility of the University of Arkansas. The equipment is configured according to the setup shown in Figure 6.1. Before performing a high-power test, a low-power test at 250 kHz frequency is needed to check all converter functionalities. Table 6.1 shows input and output parameters at low power.

Parameters	Input	Output	Efficiency
Voltage (V)	32.32	25.76	
Current (A)	1.804	2.022	
Power (W)	58.3052	52.08672	89.35%

Table 6.1 Low power test parameter

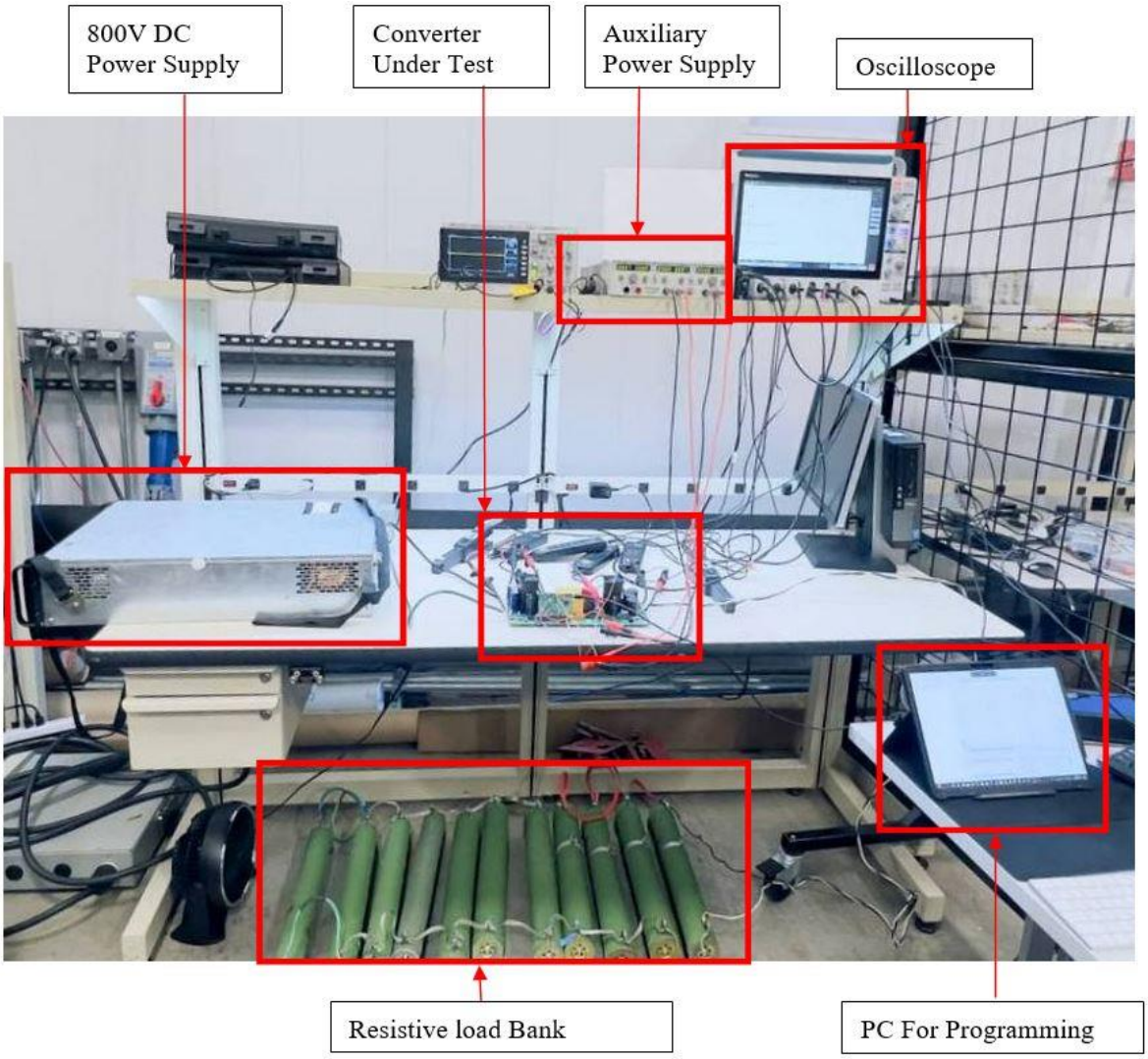


Figure 6.2 Test setup in NCREPT facilities

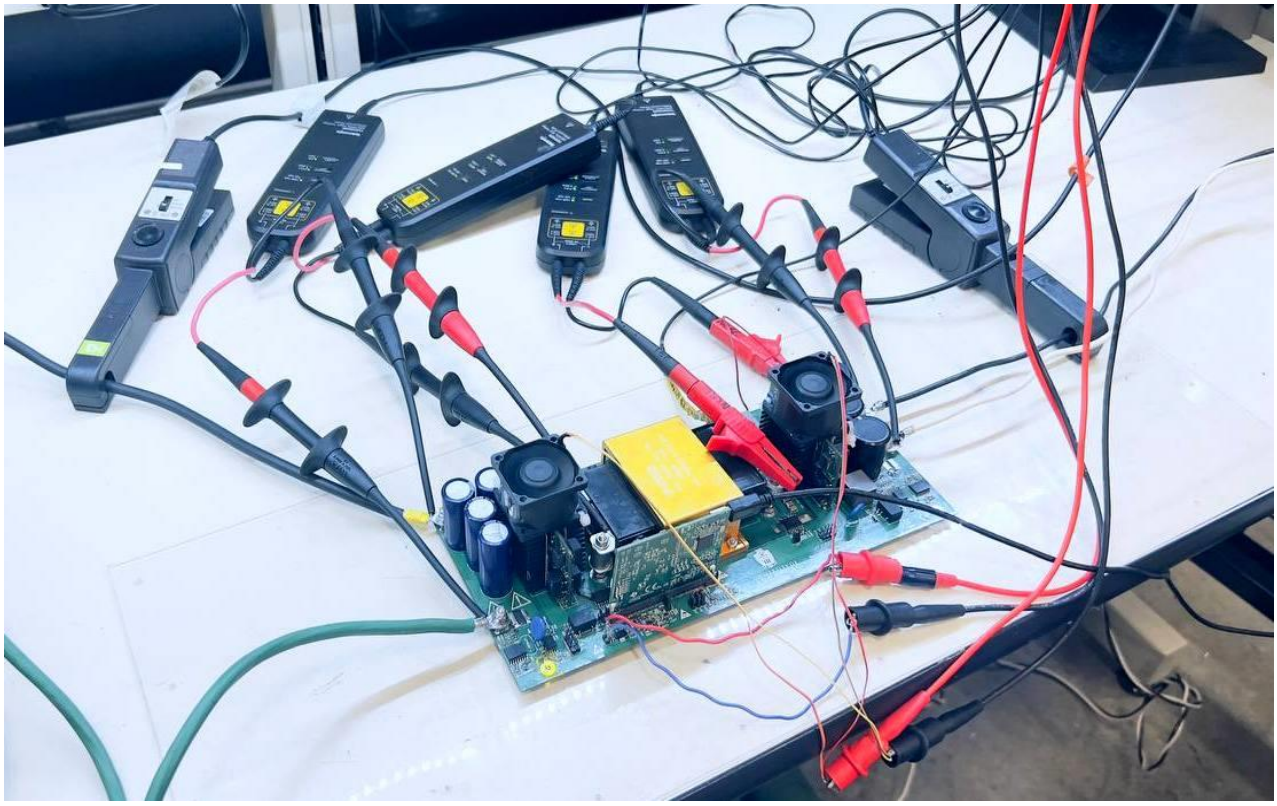


Figure 6.3 Extended View of Converter Under Test

6.3 High Power Test

The high-power test setup is configured as shown in Figure 6.3; the test was conducted at 250kHz switching frequency. Figure 6.5 (a) (b) and (c) shows the oscilloscope's waveform, which includes the primary and secondary side transformer voltage, current through the leakage inductor, input/ output voltage, and current waveform at different input voltage. It can be noted that the output voltage and current are stable with very little ripple. On the other hand, Table 6.2 (a), (b), (c), and (d) shows input and output parameters.

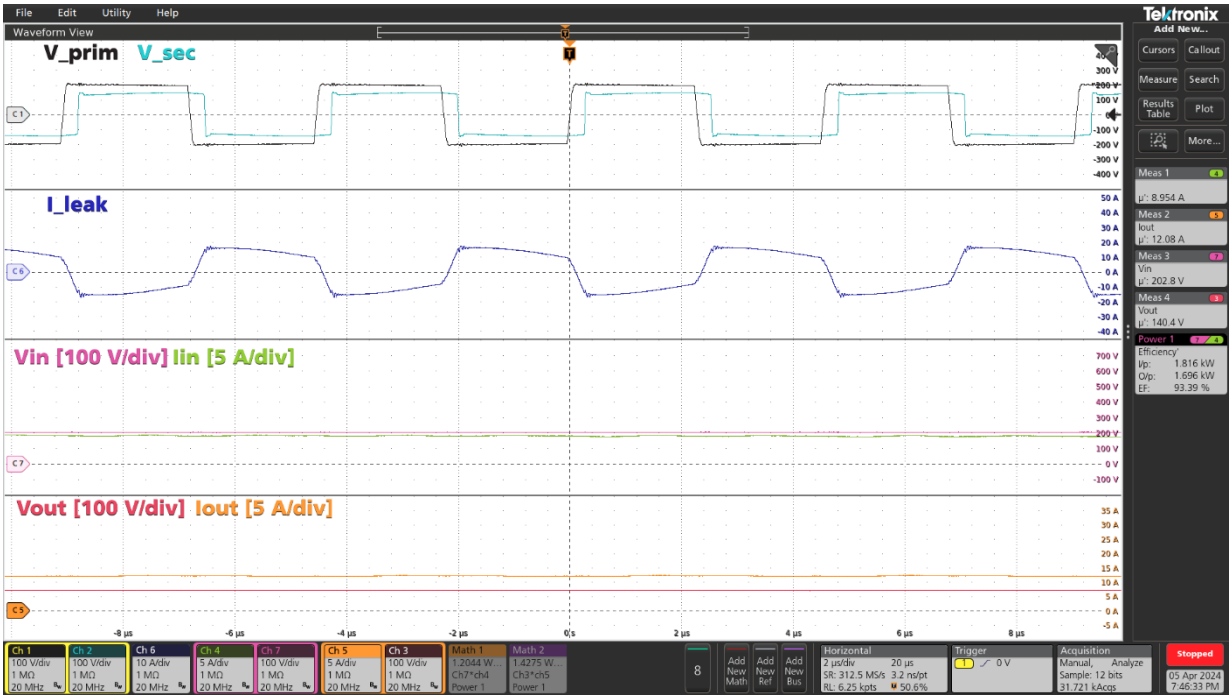


Figure 6.4 (a) Oscilloscope waveform at 202V Input voltage

Parameters	Input	Output	Efficiency
Voltage (V)	202.8	140.4	
Current (A)	8.954	12.08	
Power (W)	1816	1696	93.39%

Table 6.2 (a) High power test parameters at input voltage 202.8V

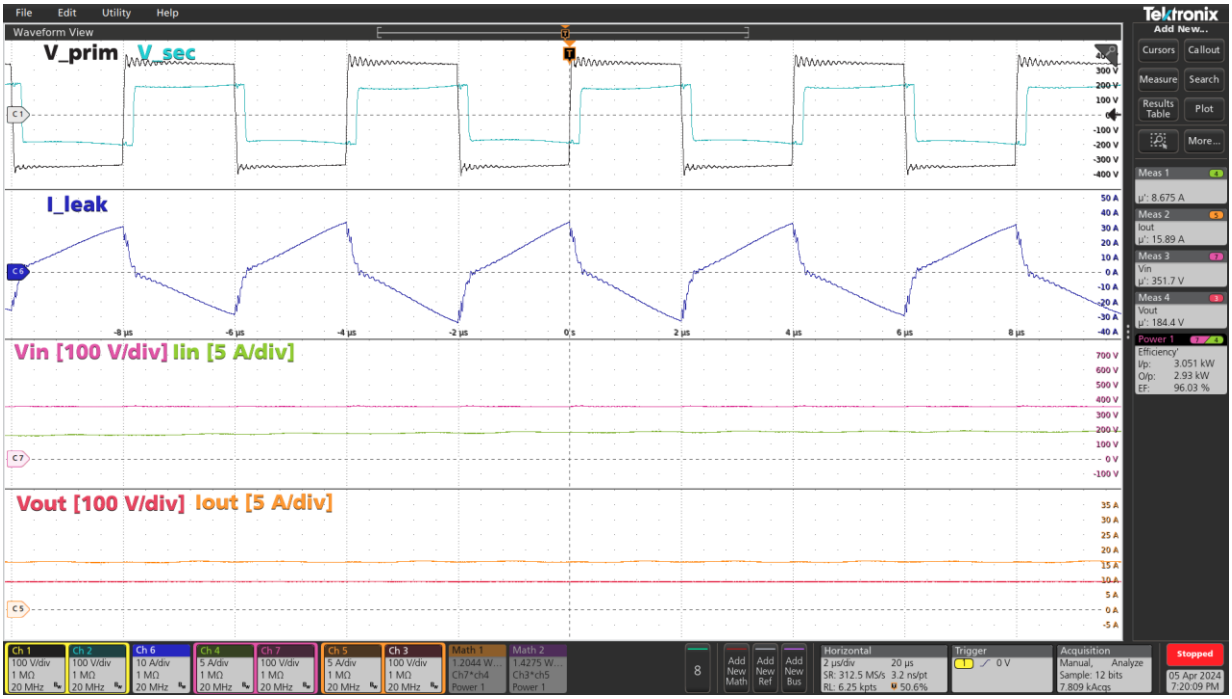


Figure 6.4 (b) Oscilloscope waveform at 351.7 V Input voltage

Parameters	Input	Output	Efficiency
Voltage (V)	351.7	184.4	
Current (A)	8.675	15.89	
Power (W)	3051	2930	96.03%

Table 6.2 (b) High power test parameters at input voltage 351.7V

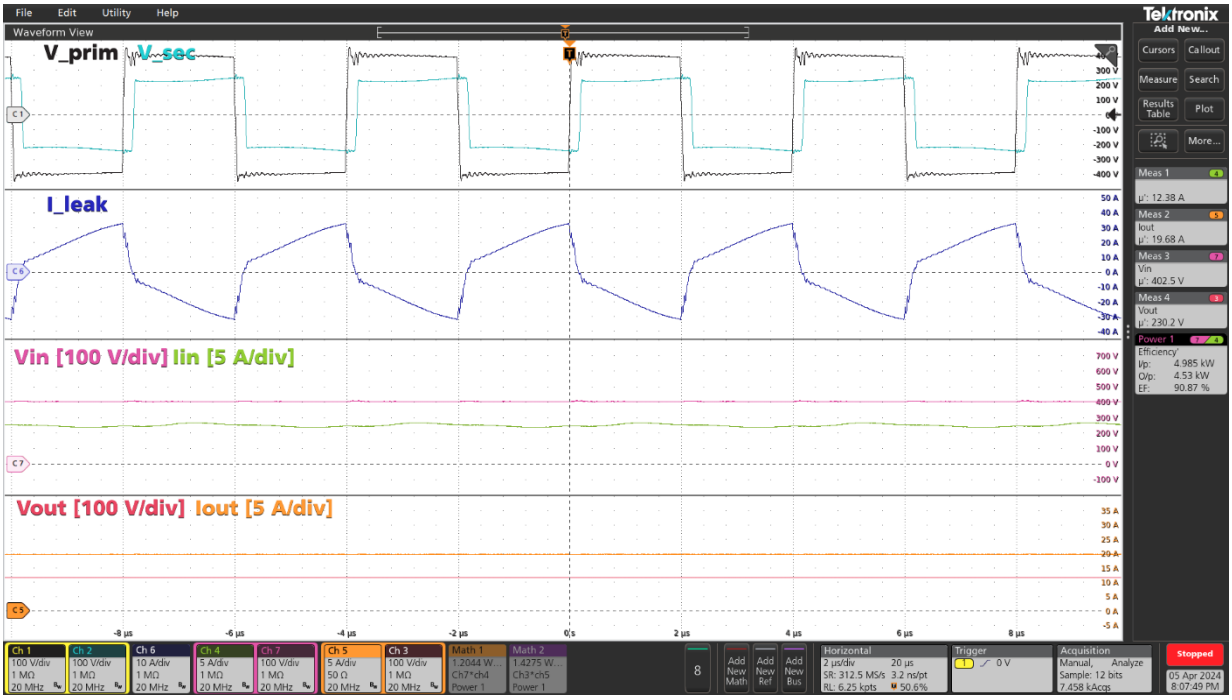


Figure 6.4 (c) Oscilloscope waveform at 402.5 V Input voltage

Parameters	Input	Output	Efficiency
Voltage (V)	402.5	230.2	
Current (A)	12.38	19.68	
Power (W)	4985	4530	90.87%

Table 6.2 (c) High power test parameters at input voltage 402.5 V

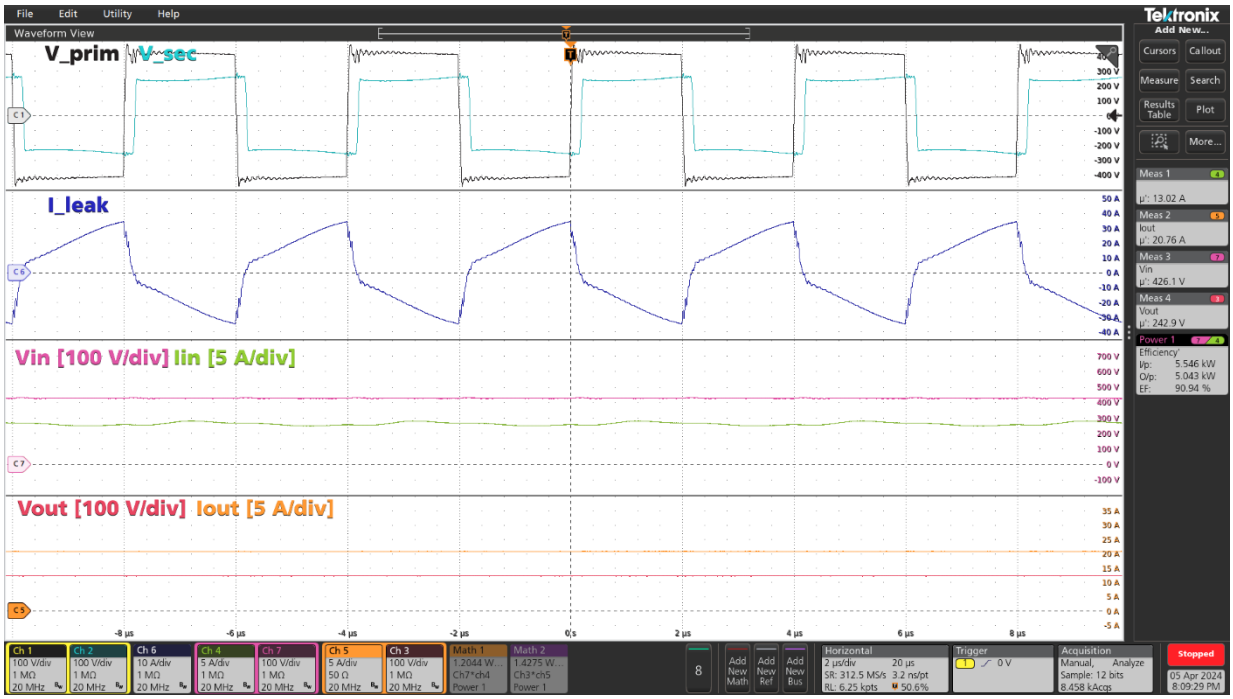


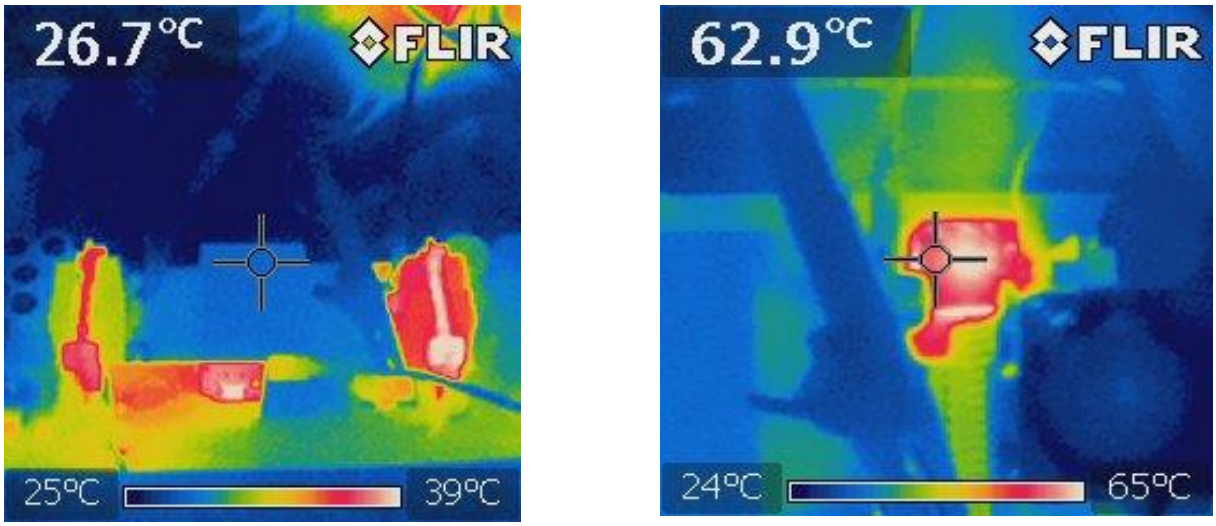
Figure 6.4 (d) Oscilloscope waveform at 426.1 V Input voltage

Parameters	Input	Output	Efficiency
Voltage (V)	426.1	242.9	
Current (A)	13.02	20.76	
Power (W)	5546	5043	90.94%

Table 6.2 (c) High power test parameters at input voltage 426.1 V

6.4 Thermal tests

FLIR's Infrared Camera was used to check the thermal performance of a DC-DC converter. The maximum temperature found was 39 degrees Celsius when the converter was operating between input 350 to 450 Voltage, as shown in Figure 6.5 (a). On the other hand, Figure 6.5 (b) shows the temperature of the energy inductor.



(a) Infrared picture of the converter (b) Infrared picture of energy inductor

Figure 6.5 Infrared picture of the converter under test

CHAPTER 7

CONCLUSION AND FUTURE WORK

7.1 Conclusion

The dissertation analyzed high-frequency bidirectional dual active bridge converter topology for electric vehicle charging applications using GaN-based power modules. GaN power modules offer high switching frequency, making them suitable for designing high-density, high-efficiency power converters. Still, at the same time, due to their high-frequency switching speed, challenges come during their implementation. The purpose of the presented work was to research the influence of leakage inductance on GaN power modules and the capability to decrease high voltage spikes and ringing. This dissertation work included designing and developing the GaN-based full-bridge power modules of 650 V and 60 A, Designing and developing a high-frequency DC-DC converter using these GaN-based power modules, and Implementing DSP coding to operate at its peak to get high efficiency.

This thesis discusses previous work where GaN-based half bridge Multichip power module and how to improve the design for present applications. A Network analyzer extracts the frequency transformer's leakage inductance and mutual inductance parameters. At the same time, analysis is done to select the suitable leakage inductance for the desired power transfer. A fair comparison has been made between SiC and GaN power switches for high-frequency applications. A mathematical analysis was done to find the specifications of components needed to design a new GaN-based power module and dual active bridge.

The work was associated with design challenges, such as designing high-frequency PCBs to reduce EMI, improve signal integrity, calibrate digital sensors, and integrate a Digital PI controller with DSP coding. The simulation uses PLECS software to analyze the various parameters for hardware design. It also includes a thermal simulation to analyze heat dissipation for proper heat sink design. A hardware prototype was built and tested using simulation, mathematical analysis, and DSP coding.

The test includes low-power and high-power tests, with the results of 5.043 kW with 90.94% efficiency. The GaN module temperature below 50 degrees indicated correct thermal work. Hence, the contributed results of the dissertation contain the requirements for the designed power electronics and the possibility of further application for EV charging purposes. This thesis underlined the necessity and problem-solving of high-efficiency applications in the hardware, coding, and thermal simulation requirements for further efficient and secure application.

7.2 Future work

The primary future work for this project could be to apply the CLLC configuration in the PCB design of this converter. The CLLC is another topology, like the dual-active bridge, which can have comparatively better efficiency. This would require re-designing the software to adjust to how the CLLC configuration would work. On the other hand, due to the measurements used to formulate primary and secondary tank currents, input/output voltages, and currents, these measurements are also required to apply control strategies in CLLC setup. Therefore, integrating the measurements used in the actual design would be a step toward designing the converter for the traditional CLLC setup. In the current design, the ADC signal is used to control the output voltage, limiting the functionality of this design to voltage regulation. However, the insertion of the triangular modulation

technique would also allow the use of ADC in current control, aiding in the operation of the inductor with Zero current switching mode. Therefore, it will ensure low power dissipation and increased efficiency, which would allow other loading capabilities up to the converter since it would perform flawlessly. Generally, future work would extend the converter design to implement the CLLC topology, integrate powers, and implement the triangular modulation.

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APPENDIX [A]

MATLAB Code for measuring leakage inductance

```
L_open_primary = 334e-6; % in Henries Lm (open Sec)
L_open_secondary = 148e-6; % in Henries (open Pri)

L_short_primary = 1.5e-6; % in Henries
L_short_secondary = 330e-9; % in Henries

turns_ratio = sqrt(L_open_primary / L_open_secondary);

L_reflected_secondary_to_primary = L_open_secondary * turns_ratio^2;
L_reflected_pri_to_sec = L_open_primary * turns_ratio^2;

L_leakage_primary = (L_reflected_secondary_to_primary *1e-6) + L_short_primary;
L_leakage_secondary = (L_reflected_pri_to_sec*1e-6) + L_short_secondary;

fprintf('Magnetizing Inductance : %f uH\n', L_open_primary*1e6);
fprintf('Turns ratio : %f uH\n', turns_ratio);
fprintf('L_reflected_secondary_to_primary: %f uH\n', L_reflected_secondary_to_primary);
fprintf('L_reflected_pri_to_sec: %f uH\n', L_reflected_pri_to_sec);
fprintf('Leakage Inductance on Primary Side: %f uH\n', L_leakage_primary*1e6);
fprintf('Leakage Inductance on Secondary Side: %f uH\n', L_leakage_secondary*1e6);
```

APPENDIX [B]

DSP code to generate ePWM signals

```
#include "F28x_Project.h"
#include "driverlib.h"
#include "device.h"
#include <stdio.h>
#include <math.h>
#include <stdint.h>
#include <file.h>

float fr = 500;
void EPWM_init();
//
// Function Prototypes
//
void PinMux_init_1();
void PinMux_init_2();
void pwm_init_C1(void);
void pwm_init_C2(void);

void main(void)
{

Device_init();
Device_initGPIO();
PinMux_init_1();
PinMux_init_2();
pwm_init_C1();
pwm_init_C2();
while(1){

}
}
void pwm_init_C1()   // ePWM1 function
{
EALLOW;
CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 0;
EDIS;
EPwm1Regs.TBPRD = fr;       // 500
EPwm1Regs.TBPHS.bit.TBPHS = 0x0000; // Phase is 0
// Setup counter mode
EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up and down
EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;        // Disable phase loading
EPwm1Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO; // Sync down-stream module
```

```
EPwm1Regs.CMPA.bit.CMPA = fr/2;    // Set compare A value
EPwm1Regs.CMPB.bit.CMPB = fr/2;    // Set compare A value
EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;      // Clock ratio to SYSCLKOUT
EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;          // Set PWM1A on Zero
EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;
EPwm1Regs.AQCTLB.bit.CBD = AQ_SET;          // Set PWM1A on Zero
EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;
// DB working fine here
EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active Hi complementary
EPwm1Regs.DBFED.bit.DBFED = fr/50; // FED = 20 TBCLKs
EPwm1Regs.DBRED.bit.DBRED = fr/50; // RED = 20 TBCLKs
EALLOW;
CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 1;
EDIS;

}
void pwm_init_C2() // ePWM2 function
{

EALLOW;
CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 0;
EDIS;
EPwm2Regs.TBPRD = fr;          // Set timer period 801 TBCLKs
EPwm2Regs.TBPHS.bit.TBPHS = fr;  // Phase angle
// Setup counter mode
EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up and down
EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE;       // Disable phase loading
EPwm2Regs.TBCTL.bit.PHSDIR = TB_DOWN; // Count DOWN on sync (=  deg)
EPwm2Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
EPwm2Regs.CMPA.bit.CMPA = fr/2;    // Set compare A value
EPwm2Regs.CMPB.bit.CMPB = fr/2;    // Set compare A value
EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;      // Clock ratio to SYSCLKOUT
EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm2Regs.AQCTLA.bit.CAU = AQ_SET;          // Set PWM1A on Zero
EPwm2Regs.AQCTLA.bit.CAD = AQ_CLEAR;
EPwm2Regs.AQCTLB.bit.CBD = AQ_SET;          // Set PWM1A on Zero
EPwm2Regs.AQCTLB.bit.CBU = AQ_CLEAR;
// DB working fine here
EPwm2Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active Hi complementary
EPwm2Regs.DBFED.bit.DBFED = fr/50; // FED = 20 TBCLKs
EPwm2Regs.DBRED.bit.DBRED = fr/50; // RED = 20 TBCLKs
EALLOW;
```

```
CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 1;
EDIS;
}

void PinMux_init_1()
{
EALLOW;
GpioCtrlRegs.GPAPUD.bit.GPIO0 = 0;    // Disable pull-up on GPIO0 (EPWM1A) pin 80
GpioCtrlRegs.GPAPUD.bit.GPIO1 = 0;    // Disable pull-up on GPIO1 (EPWM1B) pin 79
GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 1;   // Configure GPIO0 as EPWM1A    pin 80
GpioCtrlRegs.GPAMUX1.bit.GPIO1 = 1;   // Configure GPIO1 as EPWM1B    pin 79
EDIS;
}


void PinMux_init_2()
{
EALLOW;
GpioCtrlRegs.GPAPUD.bit.GPIO2 = 0;    // Disable pull-up on GPIO0 (EPWM1A) pin 76
GpioCtrlRegs.GPAPUD.bit.GPIO3 = 0;    // Disable pull-up on GPIO1 (EPWM1B) pin 75
GpioCtrlRegs.GPAMUX1.bit.GPIO2 = 1;   // Configure GPIO0 as EPWM1A    pin 76
GpioCtrlRegs.GPAMUX1.bit.GPIO3 = 1;   // Configure GPIO1 as EPWM1B    pin 75
EDIS;
}
```

APPENDIX [C]

PLCES Initialization Script

```
type_evm = 'TI280049C'; % TI280049C Piccolo Launchpad

% Configure I/O based on processor
switch (type_evm)
case 'TI28379LP'
SysClkMHz = 190;
% Configuration for TI28379D Launchpad
% on the controller side
ADC_DSP_Io = 4;
ADC_DSP_Vdc = 5;
PWM_DSP_PWM = 1;
DO_DSP_LED = 34;
DI_DSP_En = 124;
PWR_DSP_Power = 66;
SCI_DSP = [43, 42];
case 'TI280049C'
SysClkMHz = 100;
% Configuration for TI280049C Launchpad
% on the controller side
ADC_DSP_Io = 3;
ADC_DSP_Vdc = 6;
PWM_DSP_PWM = 6;
DO_DSP_LED = 34;
DI_DSP_En = 58;
PWR_DSP_Power = 56;
SCI_DSP = [28, 29];
case 'TI28379CC'
SysClkMHz = 190;
% Configuration for TI28379D Controlcard
% on the controller side
ADC_DSP_Io = 2;
ADC_DSP_Vdc = 3;
PWM_DSP_PWM = 1;
DO_DSP_LED = 34;
DI_DSP_En = 40;
PWR_DSP_Power = 39;
SCI_DSP = [28, 29];
case 'TI28388D'
SysClkMHz = 190;
% Configuration for TI28388D Controlcard
% on the controller side
ADC_DSP_Io = 2;
ADC_DSP_Vdc = 3;
```

```
PWM_DSP_PWM = 1;
DO_DSP_LED = 34;
DI_DSP_En = 40;
PWR_DSP_Power = 39;
SCI_DSP = [28, 29];
otherwise
error('Unknown evaluation module selection, please choose either "TI28379LP", "TI280049C",
"TI28379CC" or "TI28388D".')
end
f = 250e3; % switching frequency (Hz)
% Circuit parameters
Vin = 400; % input voltage (V)
Vout = 250; % output voltage (V)
Pinitial = 2500; % output power (W)
Pfinal = 2500; % output power (W)
Lm=160e-6;
Llk = 2.052e-6; % energy transfer inductance (H)
Co = 30e-6; % output capacitance (F)
Co_esr = 3.2e-3; % output capacitance ESR (ohms)
n = 2; % transformer turn ratio
Rload = Vout^2/Pinitial; % load resistance (ohms)
% Digital PI controller
Kp = 0.11173*0.015; % proportional gain
Ki = 0.11173; % integral gain
Kd = 0; % derivative gain
N = 0;
Ts = 50/f; % sample time (s)
b0 = Kp*(1+N*Ts) + Ki*Ts*(1+N*Ts) + Kd*N;
b1 = -(Kp*(2+N*Ts) + Ki*Ts + 2*Kd*N);
b2 = Kp + Kd*N;
a0 = 1+N*Ts;
a1 = -(2+N*Ts);
a2 = 1;
% Payton T250-4-16 transformer, material: TP4A
n_pri = 8; % number of turns on the primary side
n_sec = 4; % number of turns on the secondary side
Ae = 229e-6; % cross-sectional area (m^2)
Le = 60e-3; % length of flux path (m)
B_sat = 510e-3; % saturation magnetic flux denisty (T)
H_sat = 1194; % saturation magnetic field strength (A/m)
u0 = 4*pi*1e-7; % permeability of free space (m*kg*s^-2*A^-2)
ur_init = 2400; % unsaturated relative permeability
ur_sat = 4; % saturated relative permeability - tangential slope of the BH curve at Hsat
t_init = 25; % initial temperature (C)
```

APPENDIX [D]

DSP code for EV charger

```
//Code written by Rahul Biswash//

//https://www.linkedin.com/in/rahul-biswash //

#include "F28x_Project.h"
#include "driverlib.h"
#include "device.h"
#include <stdio.h>
#include <math.h>
#include <stdint.h>
#include <file.h>
//#define ADC_MODCLK 0x3 // HSPCLK = SYSCLKOUT/2*ADC_MODCLK2 = 150/(2*3) = 25.0 MHz
float Vref = 200;              // Reference  Output Voltage
double Pi = 3.141592654;
double  sysclk = 100E6;  // 100Mhz is clock frequency of F280049C
double  Freq = 250E3;     // 250khz is clock frequency of F280049C
double PWM_TBPRD ;
double Pi_inv = 1/3.141592654;
// Globals Variables
uint16_t Adc_Result_1, Adc_Result_2,
Adc_Result_3,Adc_Result_4,Adc_Result_5,Adc_Result_6,Adc_Result_7 ;
uint16_t V_input, V_output , I_input, I_in_raw, I_in_raw2, I_output, I_out_raw, I_out_raw2,
Adc_raw5, Adc_raw6, Adc_raw7 ;
// ADC Variable
float Vp_max = 0;
float Vs_max = 0;
float I_volt_max = 3300;
float Ip_ADC_value = 3300;
float Is_ADC_value = 3220;
// PID Variables
float Ts = 0;
float b0 = 0;
float b1 = 0;
float b2 = 0;
float a0 = 0;
float a1 = 0;
float a2 = 0;
float A1 = 0;
float A2 = 0;
float B0 = 0;
float B1 = 0;
float B2 = 0;
float x = 0; // computational variable
```

```
float delta0 = 0; // delta[k]
float delta1 = 0; // delta[k-1]
float delta2 = 0; // delta[k-2]
float error0 = 0; // error[k]
float error1 = 0; // error[k-1]
float error2 = 0; // error[k-2]
float delta_inv = 0;
float Pid_phase1;
float Pid_phase2;
float Pid_phase3;
// Variables for PID Controller
float Kp = 0.11173*0.06; // proportional gain
float Ki = 0.11173; // integral gain
float Kd = 0; // derivative gain
float N =  0;// derivative filter coefficient (equal to 0 when using PI control)
float cycledelay = 2; // number of pwm cycles per sample

float Adc_MAX;
// Function Prototypes
void PinMux_init();
void pwm_init_C(uint32_t raw, double tbprd, uint32_t dbfed, uint32_t dbred) ;
void PID();
void ConfigADC(void);
void initADCSOC(void);
void main(void)
{
PWM_TBPRD = (sysclk/Freq)/2;  // TBPRD = 200
uint16_t phase_CL = PWM_TBPRD/2;
//InitGpio();
Adc_Result_1=0;
Adc_MAX=4096;   // 12 bit ADC
Vp_max = 719.39;  // 719.39v maximum reading at 3.3v ADC sensor output
Vs_max = 452.5;    //  452.5v  maximum reading at 3.3v ADC sensor output
I_out_raw2 = 0;
Device_init();
Device_initGPIO();
// Configure the ePWM
PinMux_init();
InitSysCtrl();
Interrupt_initModule();
Interrupt_initVectorTable();
DINT;
InitPieCtrl();
IER |= M_INT1; // Enable CPU Interrupt 1
IER = 0x0000;
IFR = 0x0000;
```

```
InitPieVectTable();
//SysCtl_disablePeripheral(SYSCTL_PERIPH_CLK_TBCLKSYNC);
SysCtl_enablePeripheral(SYSCTL_PERIPH_CLK_TBCLKSYNC);
// Configure the ADC and power it up
ConfigADC();
// Setup the ADC for ePWM triggered conversions on channel 1
initADCSOC();
// PID Constants
Ts = 10/Freq;// Sampling Time  (0.00004)
b0 = Kp*(1+N*Ts) + Ki*Ts*(1+N*Ts) + Kd*N;
b1 = -(Kp*(2+N*Ts) + Ki*Ts + 2*Kd*N);
b2 = Kp + Kd*N;
a0 = 1+N*Ts;
a1 = -(2+N*Ts);
a2 = 1;
A1 = -(a1/a0);
A2 = -(a2/a0);
B0 = b0/a0;
B1 = b1/a0;
B2 = b2/a0;
while(1)
{
// Convert, wait for completion, and store results
ADC_forceSOC(ADCA_BASE, ADC_SOC_NUMBER0);
ADC_forceSOC(ADCA_BASE, ADC_SOC_NUMBER1);
ADC_forceSOC(ADCA_BASE, ADC_SOC_NUMBER2);
ADC_forceSOC(ADCA_BASE, ADC_SOC_NUMBER3);
ADC_forceSOC(ADCA_BASE, ADC_SOC_NUMBER4);
ADC_forceSOC(ADCA_BASE, ADC_SOC_NUMBER5);
ADC_forceSOC(ADCA_BASE, ADC_SOC_NUMBER6);
// ADC_forceSOC(ADCA_BASE, ADC_SOC_NUMBER4);
while(ADC_getInterruptStatus(ADCA_BASE, ADC_INT_NUMBER1) == false)
{
}
ADC_clearInterruptStatus(ADCA_BASE, ADC_INT_NUMBER1);
////          // Store results
Adc_Result_1= ADC_readResult(ADCARESULT_BASE, ADC_SOC_NUMBER0);
Adc_Result_2= ADC_readResult(ADCARESULT_BASE, ADC_SOC_NUMBER1);
Adc_Result_3= ADC_readResult(ADCARESULT_BASE, ADC_SOC_NUMBER2);
Adc_Result_4= ADC_readResult(ADCARESULT_BASE, ADC_SOC_NUMBER3);
Adc_Result_5= ADC_readResult(ADCARESULT_BASE, ADC_SOC_NUMBER4);
Adc_Result_6= ADC_readResult(ADCARESULT_BASE, ADC_SOC_NUMBER5);
Adc_Result_7= ADC_readResult(ADCARESULT_BASE, ADC_SOC_NUMBER6);
// Adc_Result_3= ADC_readResult(ADCARESULT_BASE, ADC_SOC_NUMBER4);
V_input    = (Adc_Result_1 * Vp_max) /Adc_MAX; // Input voltage
V_output   = (Adc_Result_2 * Vs_max) /Adc_MAX; // Output voltage
```

```
error0 =  Vref  - V_output;
delta0 = (A1*delta1 + A2*delta2 + B0*error0 + B1*error1 + B2*error2);
delta_inv = 0;
error1 = error0;
error2 = error1;
delta1 = delta0;
delta2 = delta1;
if (delta0 >= Pi*0.25)
{
delta0 = Pi*0.50;
delta_inv = 0;
}
else if (delta0 < 0 )
{
delta0 = 0;
delta_inv = 10;
}
Pid_phase1 = delta0*Pi_inv*PWM_TBPRD;
Pid_phase2 = delta0*Pi_inv*PWM_TBPRD *13.63 ;
if(Pid_phase2 > 90)
{
Pid_phase2 = 90;
}
if(Pid_phase1 > 35)
{
Pid_phase1 = 35 ;
}
// Pid_phase3 = (PWM_TBPRD*cycledelay*0.5 + delta0*Pi_inv*PWM_TBPRD);
I_in_raw   = (Adc_Result_5 * I_volt_max) /Adc_MAX;
I_in_raw2  = (I_in_raw - Ip_ADC_value)/-60;  // in mV
I_out_raw  =  (Adc_Result_3 * I_volt_max) /Adc_MAX;
I_out_raw2 =  (I_out_raw - Is_ADC_value)/-60;  // in mV
I_input    =  I_in_raw2 /2; // with 2 m Ohm Shunt devide by 2
I_output   =  I_out_raw2; // with 1 m Ohm Shunt devide by 1
Adc_raw6 = 1 + (Adc_Result_6 * phase_CL) /Adc_MAX; // Change in deadtime
Adc_raw7 = 1 + (Adc_Result_7 * phase_CL) /Adc_MAX; // Change in deadtime
// Adc_raw2 = 101 + (Adc_Result_2 * 200) /Adc_MAX; // Change in Freq
//pwm_init_C12(0, 200, 5, 5);  // Adc_raw1 is 0 for C1
pwm_init_C(Pid_phase1, PWM_TBPRD, 20, 20); // Pid_phase1
DEVICE_DELAY_US(1); //
}
}
// initADC - Function to configure and power up ADCA.
void ConfigADC(void)
{
// Setup VREF as internal
```

```
SetVREF(ADC_ADCA, ADC_INTERNAL, ADC_VREF3P3);
EALLOW;
// Set ADCCLK divider to /4
AdcaRegs.ADCCTL2.bit.PRESCALE = 6;
// Set pulse positions to late
AdcaRegs.ADCCTL1.bit.INTPULSEPOS = 1;
// Power up the ADC and then delay for 1 ms
AdcaRegs.ADCCTL1.bit.ADCPWDNZ = 1;
EDIS;
DELAY_US(1);
}
void initADCSOC(void)
{
EALLOW;
AdcaRegs.ADCSOC0CTL.bit.CHSEL     = 0;     // A0 Pin 9 (P_vSense)
AdcaRegs.ADCSOC0CTL.bit.ACQPS     = 19;    // Sample window is 10 SYSCLK cycles
AdcaRegs.ADCSOC0CTL.bit.TRIGSEL   = 10;    // Trigger on ePWM1 SOCA

AdcaRegs.ADCSOC1CTL.bit.CHSEL     = 1;     //A1 pin 11 (S_vSense)
AdcaRegs.ADCSOC1CTL.bit.ACQPS     = 19;    // Sample window is 10 SYSCLK cycles
AdcaRegs.ADCSOC1CTL.bit.TRIGSEL   = 10;    // Trigger on ePWM1 SOCA

AdcaRegs.ADCSOC2CTL.bit.CHSEL     = 2;     // A2 pin 15 (S_iSense)
AdcaRegs.ADCSOC2CTL.bit.ACQPS     = 19;    // Sample window is 10 SYSCLK cycles
AdcaRegs.ADCSOC2CTL.bit.TRIGSEL   = 10;    // Trigger on ePWM1 SOCA

AdcaRegs.ADCSOC3CTL.bit.CHSEL     = 3;     // A3 pin 17 (1.65 V)
AdcaRegs.ADCSOC3CTL.bit.ACQPS     = 19;    // Sample window is 10 SYSCLK cycles
AdcaRegs.ADCSOC3CTL.bit.TRIGSEL   = 10;    // Trigger on ePWM1 SOCA

AdcaRegs.ADCSOC4CTL.bit.CHSEL     = 5;     // A5 pin 23  (P_iSense)
AdcaRegs.ADCSOC4CTL.bit.ACQPS     = 19;    // Sample window is 10 SYSCLK cycles
AdcaRegs.ADCSOC4CTL.bit.TRIGSEL   = 10;    // Trigger on ePWM1 SOCA

AdcaRegs.ADCSOC5CTL.bit.CHSEL     = 6;     // A6 pin 25   (P_tank)
AdcaRegs.ADCSOC5CTL.bit.ACQPS     = 19;    // Sample window is 10 SYSCLK cycles
AdcaRegs.ADCSOC5CTL.bit.TRIGSEL   = 10;    // Trigger on ePWM1 SOCA

AdcaRegs.ADCSOC6CTL.bit.CHSEL     = 9;     // A9 pin 27   (S_tank)
AdcaRegs.ADCSOC6CTL.bit.ACQPS     = 19;    // Sample window is 10 SYSCLK cycles
AdcaRegs.ADCSOC6CTL.bit.TRIGSEL   = 10;    // Trigger on ePWM1 SOCA

AdcaRegs.ADCINTSEL1N2.bit.INT1SEL = 0;     // End of SOC0 will set INT1 flag
AdcaRegs.ADCINTSEL1N2.bit.INT1E   = 1;     // Enable INT1 flag
AdcaRegs.ADCINTFLGCLR.bit.ADCINT1 = 1;     // Make sure INT1 flag is cleared
EDIS;
```

```
}
void pwm_init_C(uint32_t raw, double tbprd, uint32_t dbfed, uint32_t dbred)
{
// EPWM Module 1 config
EPwm1Regs.TBPRD = tbprd; // Period = 200
EPwm1Regs.TBPHS.bit.TBPHS = 0; // Set Phase register to zero
EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Symmetrical mode
EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE; // Phase Enable/Disable
EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1; // Clock ratio to SYSCLKOUT //
HSPCLKDIV = (1 -- 0b000)
EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1; // CLKDIV = (1 -- 0b000)
EPwm1Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO; // Sync down-stream module
EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm1Regs.AQCTLA.bit.CAU = AQ_SET; // set actions for EPWM1A
EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;
EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active Hi complementary
EPwm1Regs.DBFED.bit.DBFED = 1 + dbfed; // FED = 20 TBCLKs
EPwm1Regs.DBRED.bit.DBRED = 1 + dbred; // RED = 20 TBCLKs

// EPWM Module 2 config
EPwm2Regs.TBPRD = tbprd; // Period = 200
EPwm2Regs.TBPHS.bit.TBPHS = tbprd; //  set phase as tbprd as 200 for complimentary signals
EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Symmetrical mode
EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Slave module
EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1; // Clock ratio to SYSCLKOUT
//HSPCLKDIV = (1 -- 0b000)
EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1; // CLKDIV = (1 -- 0b000)
EPwm2Regs.TBCTL.bit.PHSDIR = TB_DOWN; // Count DOWN on sync
EPwm2Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm2Regs.AQCTLA.bit.CAU = AQ_SET; // set actions for EPWM2A
EPwm2Regs.AQCTLA.bit.CAD = AQ_CLEAR;
EPwm2Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active Hi Complementary
EPwm2Regs.DBFED.bit.DBFED = 1 + dbfed; // FED = 20 TBCLKs
EPwm2Regs.DBRED.bit.DBRED = 1 + dbred; // RED = 20 TBCLKs
```

```
EPwm1Regs.CMPA.bit.CMPA = tbprd/2; // adjust duty for output EPWM1A
EPwm2Regs.CMPA.bit.CMPA = tbprd/2; // adjust duty for output EPWM2A

// EPWM Module 3 config
EPwm3Regs.TBPRD = tbprd; // Period = 200
EPwm3Regs.TBPHS.bit.TBPHS = raw; // Phase changes
EPwm3Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Symmetrical mode
EPwm3Regs.TBCTL.bit.PHSEN = TB_ENABLE; // SLAVE module
EPwm3Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1; // Clock ratio to SYSCLKOUT //
HSPCLKDIV = (1 -- 0b000)
EPwm3Regs.TBCTL.bit.CLKDIV = TB_DIV1; // CLKDIV = (1 -- 0b000)
EPwm3Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm3Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
EPwm3Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm3Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm3Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm3Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm3Regs.AQCTLA.bit.CAU = AQ_SET; // set actions for EPWM1A
EPwm3Regs.AQCTLA.bit.CAD = AQ_CLEAR;
EPwm3Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active Hi complementary
EPwm3Regs.DBFED.bit.DBFED = 1 + dbfed;; // FED = 20 TBCLKs
EPwm3Regs.DBRED.bit.DBRED = 1 + dbred;; // RED = 20 TBCLKs
// EPWM Module 4 config
EALLOW;
SyncSocRegs.SYNCSELECT.bit.EPWM4SYNCIN = 0 ;// = EPWM1SYNCIN; Need to be synced
with EPWM4 with EPWM1
EDIS;
EPwm4Regs.TBPRD = tbprd; // Period = 200 TBCLK counts
EPwm4Regs.TBPHS.bit.TBPHS = tbprd + raw; // Phase changes
EPwm4Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Symmetrical mode
EPwm4Regs.TBCTL.bit.PHSEN = TB_ENABLE; // Slave module
EPwm4Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1; // Clock ratio to SYSCLKOUT //
HSPCLKDIV = (1 -- 0b000)
EPwm4Regs.TBCTL.bit.CLKDIV = TB_DIV1; // CLKDIV = (1 -- 0b000)
EPwm4Regs.TBCTL.bit.PHSDIR = TB_DOWN; // Count DOWN on sync
EPwm4Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm4Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; // sync flow-through
EPwm4Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm4Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm4Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm4Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on CTR=Zero
EPwm4Regs.AQCTLA.bit.CAU = AQ_SET; // set actions for EPWM2A
EPwm4Regs.AQCTLA.bit.CAD = AQ_CLEAR;
EPwm4Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active Hi Complementary
```

```
EPwm4Regs.DBFED.bit.DBFED = 1 + dbfed;; // FED = 20 TBCLKs
EPwm4Regs.DBRED.bit.DBRED = 1 + dbred;; // RED = 20 TBCLKs

EPwm3Regs.CMPA.bit.CMPA = tbprd/2; // adjust duty for output EPWM3A
EPwm4Regs.CMPA.bit.CMPA = tbprd/2; // adjust duty for output EPWM4A
}
void PinMux_init()
{
EALLOW;
GpioCtrlRegs.GPAPUD.bit.GPIO0  = 0;    // Disable pull-up on GPIO0 (EPWM1A) pin 80
GpioCtrlRegs.GPAPUD.bit.GPIO1  = 0;    // Disable pull-up on GPIO1 (EPWM1B) pin 79
GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 1;    // Configure GPIO0 as EPWM1A    pin 80
GpioCtrlRegs.GPAMUX1.bit.GPIO1 = 1;    // Configure GPIO1 as EPWM1B    pin 79

GpioCtrlRegs.GPAPUD.bit.GPIO2  = 0;    // Disable pull-up on GPIO0 (EPWM1A) pin 76
GpioCtrlRegs.GPAPUD.bit.GPIO3  = 0;    // Disable pull-up on GPIO1 (EPWM1B) pin 75
GpioCtrlRegs.GPAMUX1.bit.GPIO2 = 1;    // Configure GPIO0 as EPWM1A    pin 76
GpioCtrlRegs.GPAMUX1.bit.GPIO3 = 1;    // Configure GPIO1 as EPWM1B    pin 75

GpioCtrlRegs.GPAPUD.bit.GPIO4  = 0;    // Disable pull-up on GPIO0 (EPWM1A) pin 36
GpioCtrlRegs.GPAPUD.bit.GPIO5  = 0;    // Disable pull-up on GPIO1 (EPWM1B) pin 35
GpioCtrlRegs.GPAMUX1.bit.GPIO4 = 1;    // Configure GPIO0 as EPWM1A    pin 36
GpioCtrlRegs.GPAMUX1.bit.GPIO5 = 1;    // Configure GPIO1 as EPWM1B    pin 35

GpioCtrlRegs.GPAPUD.bit.GPIO6  = 0;    // Disable pull-up on GPIO0 (EPWM1A) pin 78
GpioCtrlRegs.GPAPUD.bit.GPIO7  = 0;    // Disable pull-up on GPIO1 (EPWM1B) pin 77
GpioCtrlRegs.GPAMUX1.bit.GPIO6 = 1;    // Configure GPIO0 as EPWM1A    pin 78
GpioCtrlRegs.GPAMUX1.bit.GPIO7 = 1;    // Configure GPIO1 as EPWM1B    pin 77
EDIS;
}
void SystemStart()
{
}
```